CURRENT SOURCE CONVERTERS FOR EXTRACTION OF POWER FROM HVAC LINES

by

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DECLARATION

This thesis is the result of my own independent work, except where otherwise stated. Other sources are acknowledged by giving explicit references. A bibliography is appended.

Signed .....

Date 2006/05/05

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ABSTRACT

Two methods to convert an AC current source to an AC voltage source are presented.

Both methods make use of a current transformer to provide energy extraction from the main system while maintaining galvanic isolation between the main system and the output system. Control is via a pulse width modulation scheme in both instances.

The first method uses a storage element to provide a DC voltage, which feeds an inverter that supplies the AC load with a voltage source. The second method does not use a storage element but is a direct AC current source to AC voltage source converter employing a current transformer. This has not been done before.

A possible application of this study is in the extraction of power from high voltage transmission lines without the conventional substation and rural grid to supply small users such as the telecommunication industry.

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GLOSSARY OF TERMS AND SYMBOLS

AC	alternating current
CT	current transformer
DC	direct current
ETRC	equal time ratio control
HVAC	high voltage alternating current
IC	integrated circuit
PAM	pulse amplitude modulated
PWM	pulse width modulation / modulator
SIT	static induction transistor
SITH	static induction thyristor
TRAFTAP	non-conventional energy tapping system utilizing a transformer
TRAFTAP1	non-conventional energy tapping system utilizing a transformer and using a storage element in the conversion process
TRAFTAP2	non-conventional energy tapping system utilizing a transformer with no energy storage in the conversion process

Chapter 1 Introduction

A problem in South Africa has arisen in areas that have high voltage networks of high power rating yet do not have the population density which justifies the installation of standard power supply systems. Another problem in these areas is the supply of power to the telecommunications establishments, which is presently being addressed mainly by means of solar power generation. A power supply of several kW would meet many of the needs.

1.1 Non-conventional capacitive coupling systems

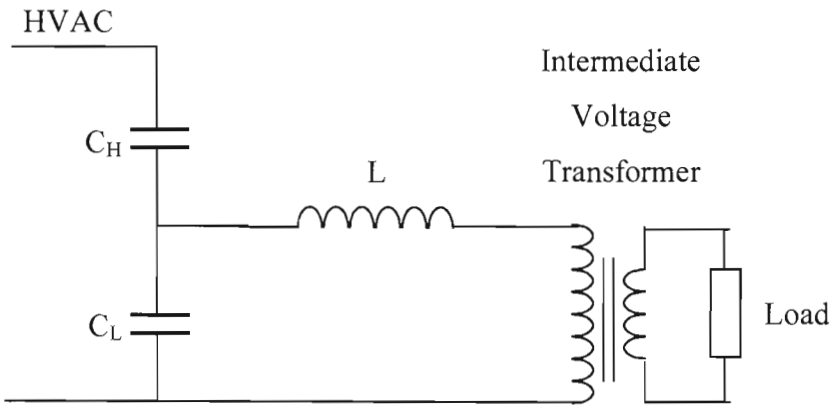


Figure 1: Basic capacitive voltage transformer circuit

There are at present in South Africa experimental capacitive coupling systems using passive series compensation where several kilometre long sections of the overhead shield wire are insulated and used to extract power. The first, with a power rating of 17 kVA, was built under supervision of Leigh Stubbs near ESKOM's Apollo substation on the Kendal Minerva transmission line in 1992 (Stubbs 1994:10, 24, 31). Referring to Figure 1, the values of this system were $C_H = 57\text{nF}$, $C_L = 124$ nF and $L = 45{,}2$ H. The second (50 kVA), using standard components, was built under supervision of Rikus Lategan in the Northern Cape a few years later (Lategan & Swart 2001:220).

The Research Institute of Hydro Quebec (I.R.E.Q.) has developed and implemented systems using capacitive coupling with varying degrees of success in Canada and in Peru. Stubbs provides a background study on these systems and their development up to the 1990's in his thesis (Stubbs 1994:2–8).

1.1.1 Overview of non-conventional HVAC extraction

The basic idea of coupling to a high voltage with a capacitive voltage divider network as shown in Figure 1 is not new. It has been used in high-voltage circuits above 66 kV. The capacitive divider circuit would provide a fairly predictable voltage if the current taken by the load would be negligible compared to the current flowing through the series connected capacitors. However, this is usually not the case. To prevent the voltage over the lower capacitor C_L from decreasing with an increasing load current, an inductor is connected in series with the load. The inductor value is such that it causes resonance at the supply frequency with the combined value of the two capacitors of the voltage divider. Further stabilization of the voltage is achieved by adding an intermediate step-down voltage transformer to further reduce the current flowing from the capacitive voltage divider (Jenkins 1967:261-263).

1.1.2 Implementation of shield wire power extraction systems world wide

Hydro-Quebec in Canada has also installed capacitively coupled tapping stations to provide power to repeater stations in telecommunications microwave links. The first were installed in 1978 and are called first generation SCC (System Capacitive Coupling). In all about 30 SCC's were installed. Due to problems such as aging, wear and tear, lightning strikes, etc, these SCC's became less reliable and also presented a maintenance problem for Hydro-Quebec. Hydro-Quebec and IREQ introduced a device during the year 2000 which they call IVACE. According to Varennes (2001), the device consists of a passive self-regulated reactive-power device based on the properties of magnetic cores with a high level of induction. It is

made up of air-gap cores over which the two primary and the two secondary windings are superimposed. These are connected to the first through a diode rectifier bridge (the device's only electronic component) and through magnetic flux. The reactor voltage regulating range is set to a pre-established level and the power rating is based on permanent needs (25 kVAR). Under these circumstances, it is reported to have excellent operating characteristics and a high level of immunity to disturbances (Varennes 2001). It is further reported that the output voltage is regulated and is a sinusoidal voltage whose amplitude is independent of the voltage of the overhead ground cable.

1.1.3 Applications of physical coupling capacitor systems

Physical coupling capacitor systems have also been developed and implemented in Peru to provide power to villages in remote areas. These system voltages are limited to 275 kV (Stubbs 1994:7-8).

1.2 Solution proposed by this research

Extraction of power from a HVAC line by means of a current transformer has not been developed, neither implemented. Two solutions proposed by this research are:

- Alternating current to DC voltage to alternating voltage conversion. (TRAFTAP1)
- Direct alternating current to alternating voltage conversion. (TRAFTAP2)

1.2.1 Alternating current to DC voltage to alternating voltage conversion

The output of a current transformer (CT) coupled to the transmission line is converted to a DC voltage in a storage element (capacitor) and then converted to an alternating voltage by means of an inverter.

1.2.2 Direct alternating current to alternating voltage conversion

The output of a current transformer is pulse width modulated to provide a regulated AC voltage without a storage element. This has not been done before.

1.3 Conventional transmission to rural grids

Typically, electric power is generated at 22 to 26 kV inside a generating station by means of alternators driven by steam turbines. An outdoor sub-station containing step-up transformers converts the alternator voltage to the transmission voltage, which can be up to 765 kV depending on the distance that it must be transmitted. At the point of usage, sub-stations containing step-down voltage transformers are used to step the voltage down to 11 kV or lower for local distribution to residential, commercial and industrial facilities (Traister 1983:7, 83).

To provide electric power to users situated far from high population density or industrial sites such as mines, a rural grid must be constructed from an existing sub-station to the location of the user. Such a rural grid costs several thousand rand per kilometre and for every doubling of the power rating the cost increases four fold. This puts electric power out of range for many rural dwellers in Southern Africa on economic grounds alone.

In many countries electric power is consumed at a great distance from the generating station. The position of the power station is dependent on an abundant source of energy for driving the turbine (water, coal, gas, oil or nuclear). The usage of electrical energy takes place in areas in which sufficient economic activity is taking place such as mining, manufacturing, intensive farming, importation/exportation of raw materials and manufactured goods. The position of the electric power station and the place where the electric power is used is therefore not necessarily in the same geographic location. This leads to long transmission lines of high voltage to minimize losses in the lines. These high voltage grid lines are constructed over vast

distances over which major transport routes also run. The telecommunication industry has repeater stations (cells) all along these routes and rely on power for the repeater mostly on solar panels which are expensive, have a short life span, are easily vandalized or stolen and also require periodic maintenance.

1.3.1 Non-conventional connection eliminates rural grid

Providing an inductive coupling via a current transformer of high voltage insulation and sufficient power rating, coupled to a current to voltage converter to supply a 50Hz 230V output from a supply line, would meet the needs of the repeater stations as previously stated. This would unlock potential for bringing more users into the electric fold which otherwise would not be economically justifiable. This method of connecting to the transmission line will eliminate the need for the conventional rural grid from a conventional substation to the rural user (Figure 2).

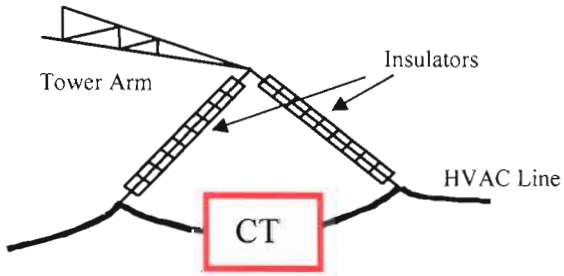


Figure 2: CT based tapping methods

1.4 Delimitations

The research excludes practical experiments on high voltage lines. Although the practical construction of a high voltage CT is excluded, aspects of the design of a high voltage CT will be addressed in this work. The research will only focus on methods that can be employed to transform an alternating current source into an alternating voltage source. Small models will be used to verify the practical

implementation of the methods. The DC-to-AC controller and PWM inverter shown in Figure 4, are not included in this research, since much has been done on these by others and would not contribute anything new.

1.5 Summary

Non-conventional tapping methods have been around for some time in the world and have been experimentally tested in South Africa. The tapping method has been of a capacitive nature. The aim of non-conventional tapping methods is to eliminate the rural grid alongside transmission lines in order to cut costs.

Two inductive tapping methods are proposed by this research:

- The output of a current transformer, inserted into a transmission line, is pulse width modulated to provide a stable DC voltage which is then fed to an inverter to provide a constant voltage fixed frequency AC supply.
- A current transformer with two secondaries is inserted into a transmission line. One secondary feeds an AC load. The other secondary feeds a switch which is pulse width modulated in such a manner as to provide a constant voltage fixed frequency AC supply to the AC load on the other secondary winding. In essence, a direct alternating current to alternating voltage converter without any storage element. This has not been done before.

The research is limited to small models of the systems in order to prove that power tapping using a current transformer is indeed possible.

Chapter 2 Current to voltage conversion with a storage element

This chapter describes the current to voltage conversion process using a capacitive storage element (TRAFTAP1). Firstly, the principle of duality is explained and then applied to help with the explanation of the unfamiliar AC current source by contrasting it with the familiar AC voltage source. Then a block diagram of the TRAFTAP1 system is introduced and each functional block is described individually. This is followed by analysis of the controller action as implemented with a UC3842 integrated circuit. This is followed by analysis of the design of the system. The simulation results and experimental results wrap up the rest of the chapter.

2.1 Theory

Electrical engineers are more familiar with voltage sources than with current sources, since that is what is usually encountered in the normal application of electrical engineering. Applying the principle of duality will greatly ease the explanation of the current transformer in this unusual application power provider.

2.1.1 The principle of duality

The principle of duality applied in electrical engineering means that if a situation viewed on a voltage basis is analogous to another situation viewed on a current basis, or vice versa, then the equations relating to one situation can be derived from those of the other merely by a routine interchange of the quantities or concepts. Thus Ohm's law may be written not only as $v = iR$, but also as $i = vG$ (Brosan & Hayden 1966:104).

The second equation is obtained from the first by interchanging voltage v, current i and by replacing resistance R by conductance G. Quantities interchanged in this way are said to be dual elements and the two equations are dual equations. In a similar

way, the equations $v = L\frac{di}{dt}$ and $i = C\frac{dv}{dt}$ are called duals (Brosan & Hayden 1966:104).

Voltage and current are once more interchanged and the inductance, L, and capacitance, C, are two new dual quantities. The virtue and justification of this procedure is that, when duals have been defined from one pair of equations, the same duals apply in another pair of equations. This has already been done above for voltage and current. By working with dual quantities it is possible to recognize that many laws of physical phenomena occur in pairs, and it becomes possible to discover new (or at least unfamiliar) relations by direct analogy. Further, when the solution of the dual of a problem is known, the solution of the problem can be written down at once (Brosan & Hayden 1966:104).

2.1.2 Applying the principle of duality

Electric power can be transferred from one circuit to another either capacitively or inductively. Inductive coupling is mainly achieved by means of voltage transformers coupled in parallel, which is the conventional way.

An alternative to capacitive coupling in the non-conventional way to the high voltage lines would be to use inductive coupling. Two alternatives are available:

- Iron Core Current Transformer
- Air Core Voltage Transformer

The current transformer is connected in series in the line. Extracting power via a current transformer does at first not seem to be a plausible alternative in any situation but as this study will reveal it can be done. The air-core voltage transformer is not the focus of this research.

Applying the concept of duality to the problem at hand it can plainly be seen that it

could well be a method of extracting power. Where a voltage transformer is connected in parallel, a current transformer is connected in series. Where a voltage transformer secondary may in normal operation never be short circuited and can safely be left open circuit, a current transformer secondary may in normal operation never be left open, but must be short-circuited to avoid potentially disastrous results.

To control the power from a voltage transformer a switch in series with the load is used. Closing this switch transfers power to the load and opening it, interrupts the flow of power to the load. The duty cycle of the switch is directly proportional to the power transferred to the load.

Applying the principle of duality, power from a current transformer is then controlled by a parallel switch, which shunts current away from the load when it is closed and transfers power to the load when it is open. The complement of the duty cycle of the switch is directly proportional to the power transferred to the load.

Table 1: Duality comparison VT versus CT

	VT	CT
Primary Circuit Connection	Parallel	Series
Secondary Side Switch in	Series	Parallel
To Transfer Power, Switch	Closed	Open
No Load, Switch	Open	Closed
Duty Cycle	D	1-D

2.1.3 The TRAFTAP1 system

Since this system has not been implemented as yet a few thoughts on the practical realization of this system would be in order. There after a description of the system

will follow.

2.1.3.1 Physical set-up of the TRAFTAP

The fact that the system consists of a high voltage and a low voltage side makes it desirable to split the system into two parts, the CT and the power converter. Both these parts must be mounted on poles to protect personnel and others from accidental contact with the system (Figure 3). Placing the two parts away from each other further protects maintenance personnel from the high voltage present at the current transformer. A pole switch placed in parallel with the CT secondary will prevent power from reaching the power converter. This will enable maintenance to take place even while the main transmission line is functional. A ground switch can also be situated in close proximity to the shunting switch to further protect maintenance personnel.

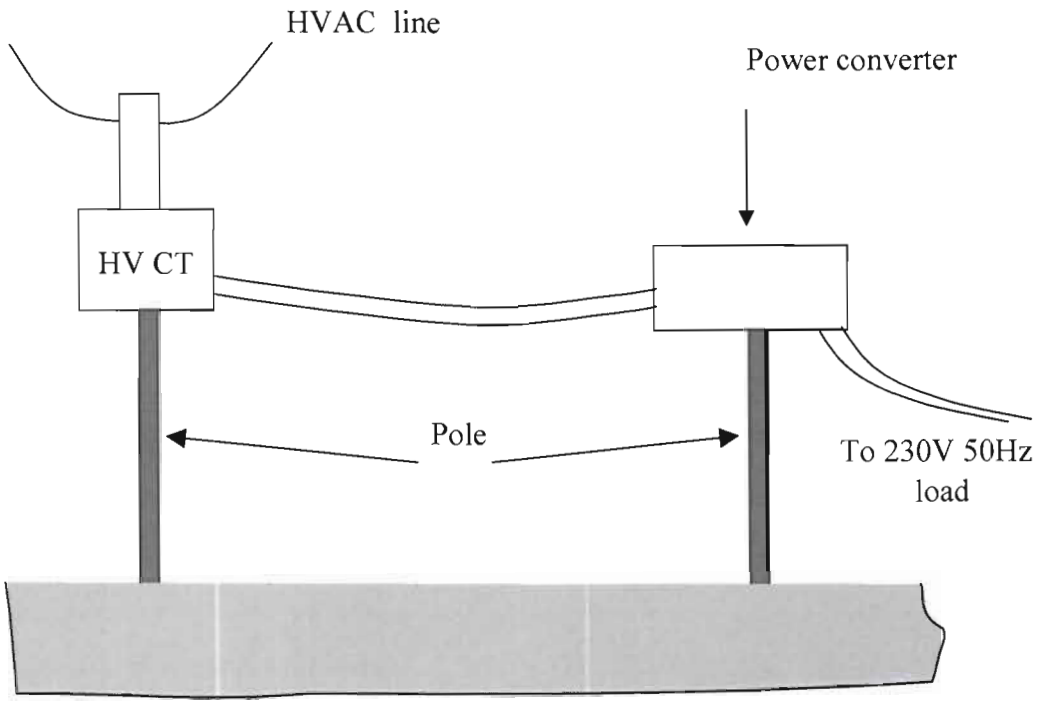


Figure 3: Physical set-up of TRAFTAP

A brief description of each of the blocks shown in Figure 4 would be appropriate at this time to familiarize the reader with the proposed system.

2.1.3.2 The current transformer (CT)

High voltage current transformers do not yet exist. The design of such a CT should consider that it is neither a measurement nor a protection CT, but must be able to deliver power. However, it should have the saturation profile of a measurement CT to enable the system to withstand any fault conditions that may arise from time to time on a transmission line. Capacitive graded bushing will have to be used to provide the necessary isolation between the high voltage line and the CT casing, which will be at earth potential. A sketch showing the capacitive graded bushing is shown in Figure 5. The sketch is a collage of sketches taken from Grigsby (2001:3-175).

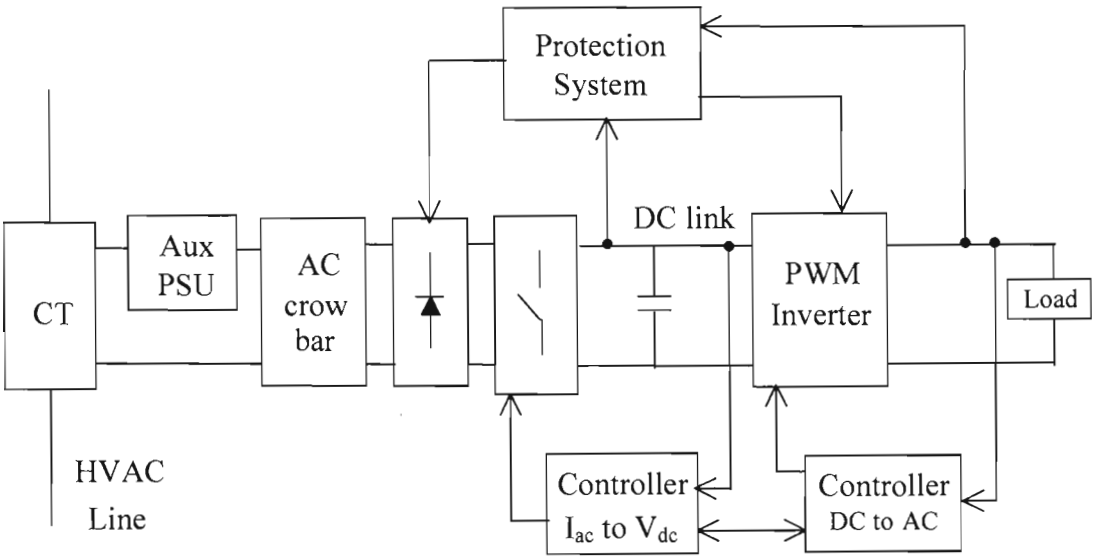


Figure 4: Block diagram of the complete TRAFTAP1 system

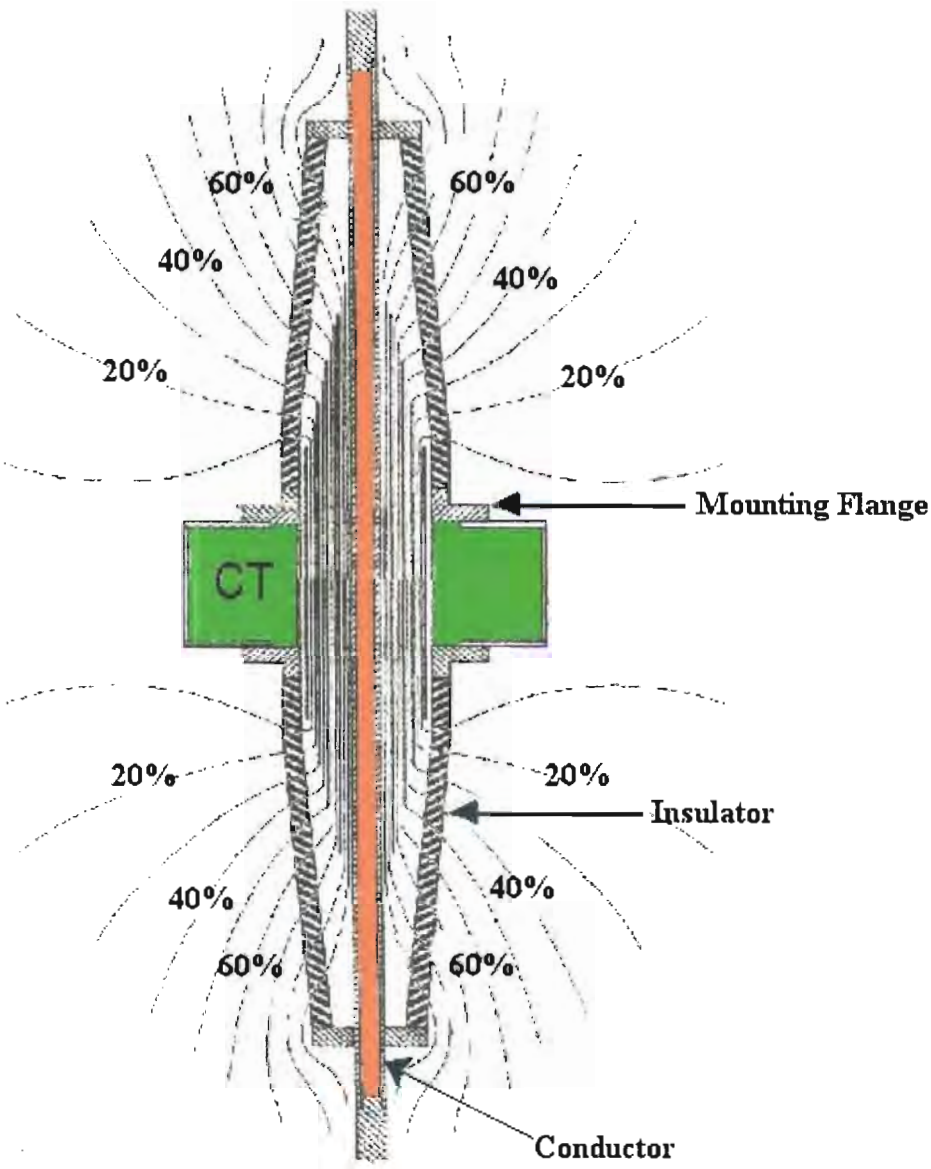


Figure 5: Illustration of proposed capacitive graded bushing for a power CT

2.1.3.3 Auxiliary power supply unit (PSU)

Since the system is connected to a high voltage transmission line, the delivery of power will be dependant on whether the power flow in the transmission line is sufficient to supply the load. Remember that the TRAFTAP1 system is drawing power in series with the actual load of the transmission line. It can be seen as a parasitic load. This implies that if the current in the transmission line falls too low,

the output current available from the CT will not be enough to sustain the power requirements of the TRAFTAP1 load.

In this scenario, the TRAFTAP1 will interrupt the power to the load by keeping the main switch closed and thereby applying a short to the CT output. However, the supply for the control and protection circuits may not be interrupted as long as there is power flowing in the high voltage transmission line since this would seriously compromise the TRAFTAP system with very destructive results. To keep the electronic switch closed will require a supply. Therefore, an auxiliary PSU is required. It is basically a miniature TRAFTAP since it has to convert an AC current to a DC voltage but at a much lower power level.

Devices that would be ideally suited as the main electronic switch in the TRAFTAP, would be the SIT (Dudrík 2001:28) or SITH (Dudrík 2001:54). These two devices are normally closed, which in the event of a failure of the auxiliary supply would automatically short the output terminals of the CT. This would satisfy the age-old requirement: "Never leave the output terminals of a CT open circuit". Although experimental devices have been developed for the SIT and SITH no commercially available devices could be found for experimental purposes. A drawback of the SIT at this time is the relatively high on-state resistance of 1,2 Ω (Rashid 2004:11). Thus, due to availability and cost, the device of choice in the experimental set-up is a MOSFET.

2.1.3.4 AC crow bar

A failure of the diode bridge or main switch causing an open circuit condition would have disastrous results in the CT. Momentary loss of control of the switch could also cause a potentially destructive situation.

An AC crow bar circuit, which would switch on a thyristor in a back-to-back configuration if the CT voltage increases beyond a predetermined safe value, would

provide the necessary protection. The thyristors would switch off at every current zero, effectively resetting the protection if the voltage control is restored. The circuit of the crowbar is shown in Figure 6. Further details of this circuit can be found in chapter 4.

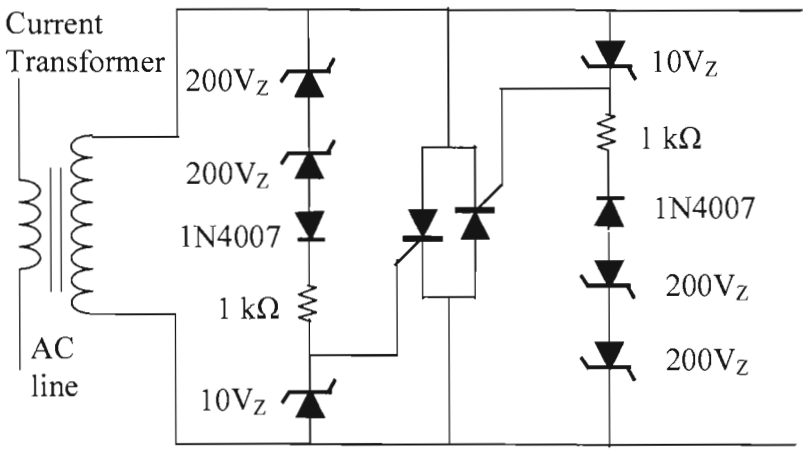


Figure 6: Detail of the AC crowbar circuit

2.1.3.5 Diode bridge

The diode bridge converts the AC current into a pulsating DC current with a frequency of twice that of the transmission line fundamental frequency (Figure 7). The diodes in the bridge do not have to be fast switching diodes since the current flowing through them is diverted either through the switch S_1 or through the boost diode towards the capacitor.

2.1.3.6 Main switch, fast-switching boost diode and DC link capacitor

The main switch S_1 effectively shorts the output of the bridge when it is closed. It must be able to carry the maximum current output that the CT can deliver continuously. When the main switch is open, the current delivered by the CT via the bridge rectifier flows through a fast-switching diode.

The CT, which experiences a higher $d\varphi/dt$ at the instant that the switch changes state (closed to open), supplies the forward bias on the diode. The diode feeds charging current to the DC link capacitor and blocks discharging of this capacitor via the main switch when it is closed again. The main switch is controlled by a PWM technique.

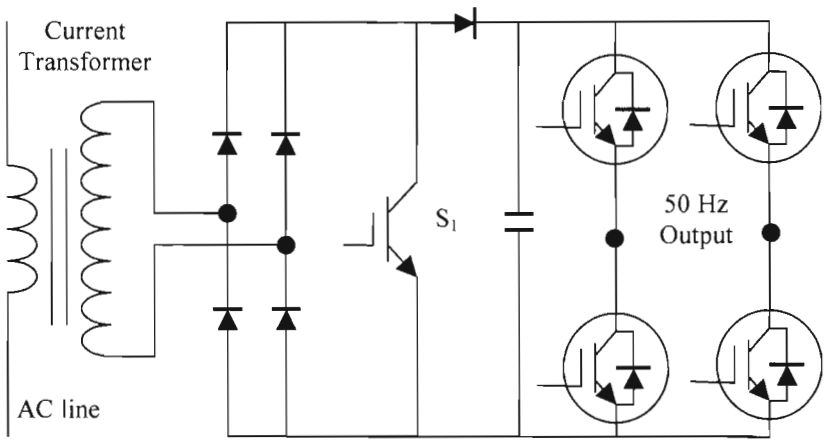


Figure 7: Basic current source to voltage source converter circuit

2.1.3.7 Current source to voltage source converter

The system front end from the CT up to the DC link is in effect a current source to voltage source converter. It is appropriate to elaborate on this converter before continuing with the description of the system. The basic current-fed system comprises simply a current transformer in series with the power system. This reduces effectively to a current source feeding the load. Since the load requires a voltage-fed system, some power electronics is required as shown in Figure 7. If one applies the duality concept, it becomes clear that the input current will then be sinusoidal, while any distortion will be in the voltage waveform.

Figure 7 shows the essential components of the circuit. There is nothing unusual

about the circuit configuration, except for the input supply. This is a current source instead of a standard voltage source. The switch S_1 comprises an IGBT or MOSFET.

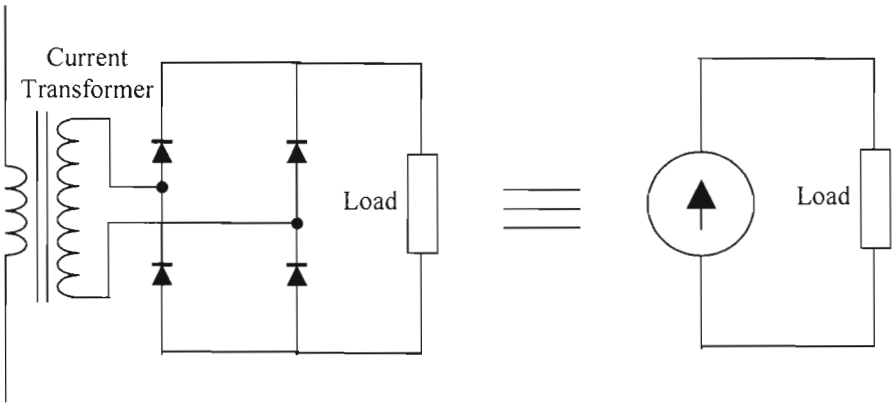


Figure 8: CT feeding a load via a rectifier and averaged equivalent circuit

Since the current transformer does not permit an open circuit, current control is carried out by means of the switch S_1 effectively across the secondary terminals of the current transformer. When the switch S_1 is off, the current from the bridge flows towards the capacitor, with the secondary transformer voltage rising to the capacitor voltage value to force the diode to conduct. When the switch S_1 is closed, the current flows through S_1 and the voltage drops to zero. In effect, this is the dual of a voltage input converter, which would have a series switch to carry out voltage control.

2.1.3.8 Averaging of the current source to voltage source converter

A CT feeding a load via a rectifier bridge can be reduced to a constant current source by averaging the circuit (Figure 8). A basic current converter can be realized by placing a parallel switch between the load and a constant current source (Figure 9.) Diverting the current through the switch S_1 away from the load will reduce the average current through the load (Mitchell 1988:14).

The average of the output current I_2 is now a function of the duty cycle D of the

switch:

$$I_{2ave} = (1 - D)I_1 \tag{1}$$

where I_1 is the input current from the current source.

The basic current converter can be modified to become a current to voltage converter by the addition of a capacitor in parallel to the load. From the *v-i* relation of a capacitor it can be seen that a current can be transformed into a voltage by allowing the current to flow into a capacitor. This relation is mathematically expressed as

$$v_c = V_C(0) + \frac{1}{C}\int i_C dt \tag{2}$$

where

v_c is the instantaneous capacitor voltage,

$V_C(0)$ is the initial capacitor voltage,

i_C is the instantaneous capacitor current and

C is the capacitor value in Farad.

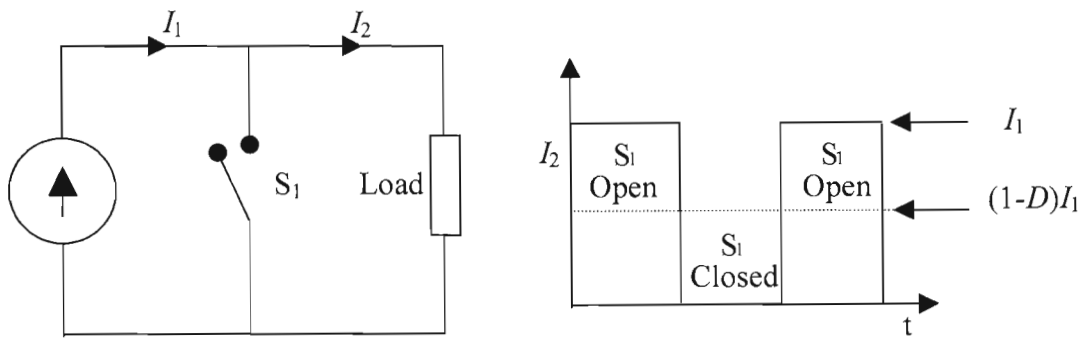


Figure 9: Basic current converter

However, it is not permitted to place a switch in parallel with a capacitor due to the infinite current that is created on closure of the switch (Agrawal 2001: 25); (Mitchell 1988:14). This means that a switch must be placed between the capacitor and the parallel switch (Figure 10). This switch must be OFF when the parallel switch is ON to prevent an infinitely high current via the parallel switch, which would rapidly discharge the capacitor and also possibly damage the parallel switch. Furthermore, this switch must be ON when the parallel switch is OFF to allow for charging of the capacitor according to equation (2). In practice, the switch S_2 which prevents discharge of the capacitor can be realized by a diode.

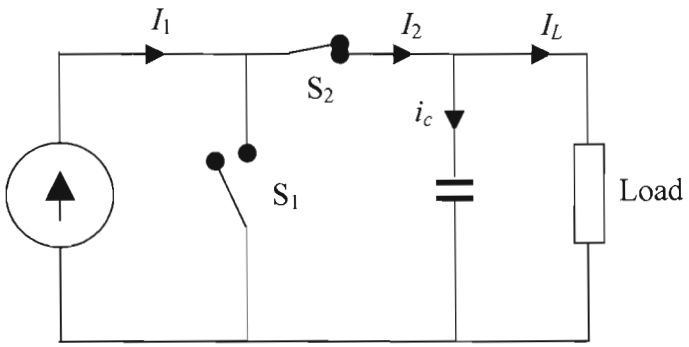


Figure 10: A basic current-to-voltage converter

Referring to Figure 10 the current flowing in the capacitor, i_c is given by:

$$i_c = I_2 - I_L \tag{3}$$

where

I_2 is the current flowing through switch S_2 (diode) and

I_L is the load current

Substituting equation (3) into (2) yields:

$$v_C = V_C(0) + \frac{1}{C}\int (I_2 - I_L)\,dt \tag{4}$$

Substituting equation (1) into (4) yields:

$$v_C = V_C(0) + \frac{1}{C}\int\left((1-D)I_1 - I_L\right)dt \tag{5}$$

From this it can be seen that the output of the current transformer can be transformed into a voltage. Further, the voltage across the capacitor can be kept constant by varying the mark-space ratio *D* (Janse van Rensburg & Case 2001:427-429).

2.1.4 Description of the complete circuit action

The internal block diagram of the UC3842 as well as the basic power circuit and feedback components are shown in Figure 11. Circuit action under two conditions is described below. The two conditions are:

- the plant (main storage capacitor) voltage has reached the set value and
- the voltage of the capacitor is below the set value.

Once the capacitor reaches its desired voltage, the current from the CT must be diverted via S_1 otherwise the capacitor voltage will continue to increase. The voltage over the capacitor is sampled by the resistive divider R_3/R_4 and applied to a PI opamp stage. This voltage should be equal to the reference voltage of 2,5 V which is internally provided by the IC to the opamp non-inverting input. Since the two inputs are equal, the output of the opamp should also be 2,5 V, since no current will be flowing through R_1 or R_2 and since C_1 is a small capacitor it should also quickly discharge to zero. A double diode volt drop reduces the output of the PI opamp circuit before being divided by 3 by the resistive voltage divider circuit formed by $2R_a$ and R_a as shown in equation (6).

$$V_{error} = \frac{V_{PI} - 2V_D}{3} \tag{6}$$

$$V_{error} = \frac{2,5 - 2(0,6)}{3} = 0,433V \quad (7)$$

The inverting input of the comparator is supplied by a ramp voltage, which must ramp up from about 0,433 V upwards to a maximum value of 1 V (the internal block diagram has a 1 V zener parallel to R_a). The comparator output will be low as long as the ramp voltage is lower than the error voltage and high as long as the ramp voltage is higher than the error voltage.

Making the assumption that the ramp voltage starting level is just below the error voltage level, this would make the PWM comparator opamp output low. This output is applied to the SR latch RESET input, which is edge trigger on a low-to-high transition.

The SET input of the latch is coupled to a synchronizing pulse, which sets the latch every time the ramp voltage period ends. Thus, the SR latch is set at the start of each ramp voltage period and reset as soon as the ramp voltage exceeds the error voltage. The SR latch $\overline{Q}$ output is logically OR-ed with the synch pulse. The output of the OR gate is used to drive a totem pole output. If any input to the OR gate is high, the lower transistor in the totem pole is switched on which drives the UC3842 output low. If both are low, the output of the IC is high. Thus the synch pulse drives the IC output low and, at the end of the synch pulse, the totem pole pulls the IC output high until the ramp voltage exceeds the error voltage. This resets the SR latch ($\overline{Q} = 1$), which pulls the IC output low.

The IC output is fed to a transistor switch, which inverts the IC output to drive the main switch S_1. Thus, as long as the ramp voltage is lower than the error voltage the main switch S_1 is ON and the moment the error voltage exceeds the error voltage S_1 is OFF, thus preventing the capacitor from being charged further.

If the plant voltage is lower than the set voltage, the voltage fed back via R3/R4

would be less than 2,5 V (Figure 12). Since the PI opamp circuit has an inverting action it would therefore have an output voltage greater than 2,5 V.

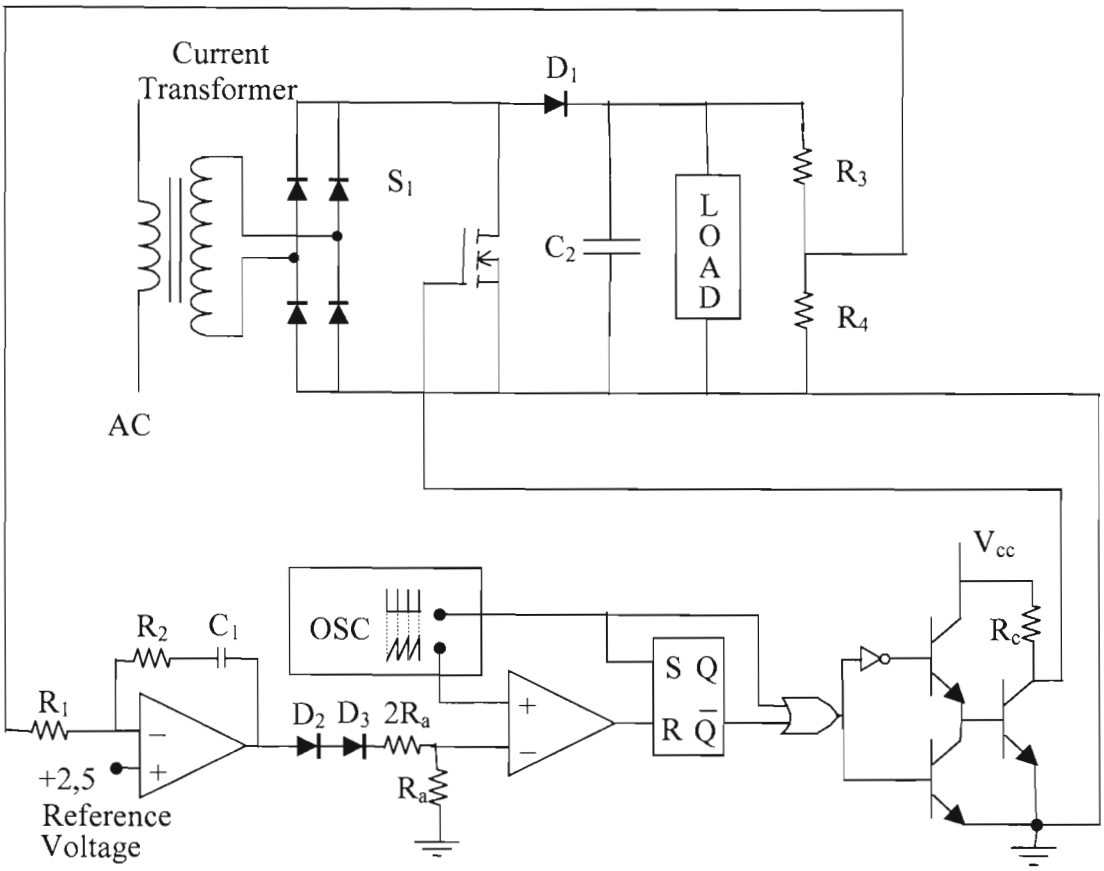


Figure 11: IC block diagram, basic power circuit and feedback components

This would mean that the error voltage would be greater than 0,433 volt. The ramp voltage would therefore be less than the error voltage for a longer time, resulting in a longer time that S_1 would be open. This would allow current to flow via the diode D_1 into the main capacitor C_2 increasing its charge and therefore its voltage and thereby reducing the error.

Figure 13 illustrates that when the error voltage is near zero the diode will be ON for the minimum of time just trickle charging the plant capacitor.

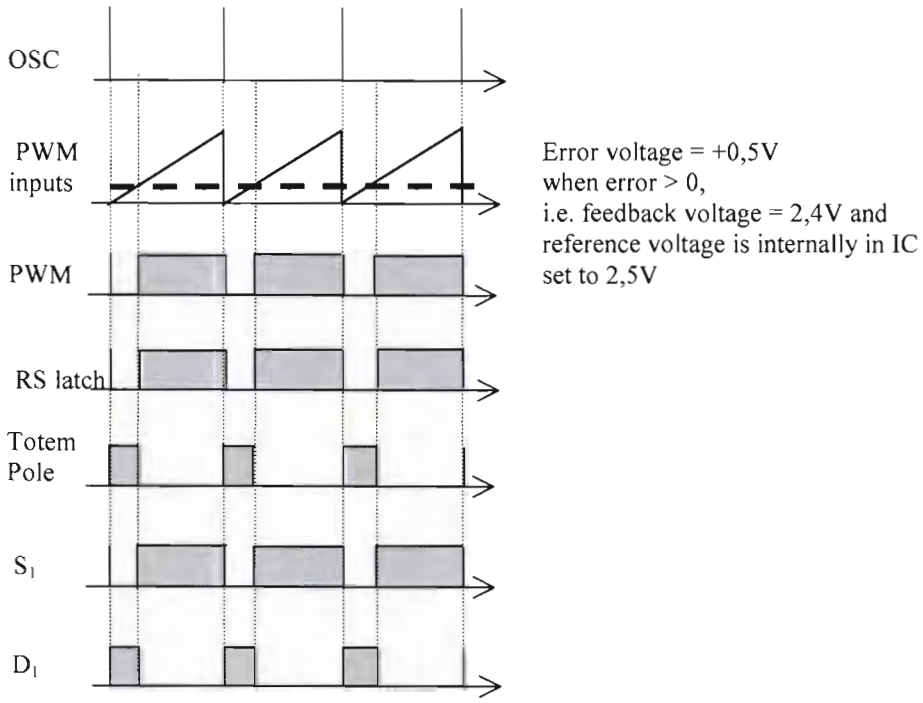


Figure 12: PWM action with error voltage greater than zero

2.2 Aspects of analysis and design

The three major objectives of system analysis and design are to

- produce the desired transient response
- reduce the steady-state error and
- achieve stability (Nise 2000:14, 38).

The PI controller is designed around a PWM controller IC UC3842. Although the IC itself is basically a current mode controller it can be used as a voltage-mode PWM controller (Unitrode 1999:3-64). The choice of the IC was based on availability since any voltage-mode PWM integrated circuit would suffice. The IC was later replaced with a UC3843 also due to availability of the UC3843 and the fact that the UC3842 were out of stock. The difference between the two types is the under voltage lockout which was not a factor in the application.

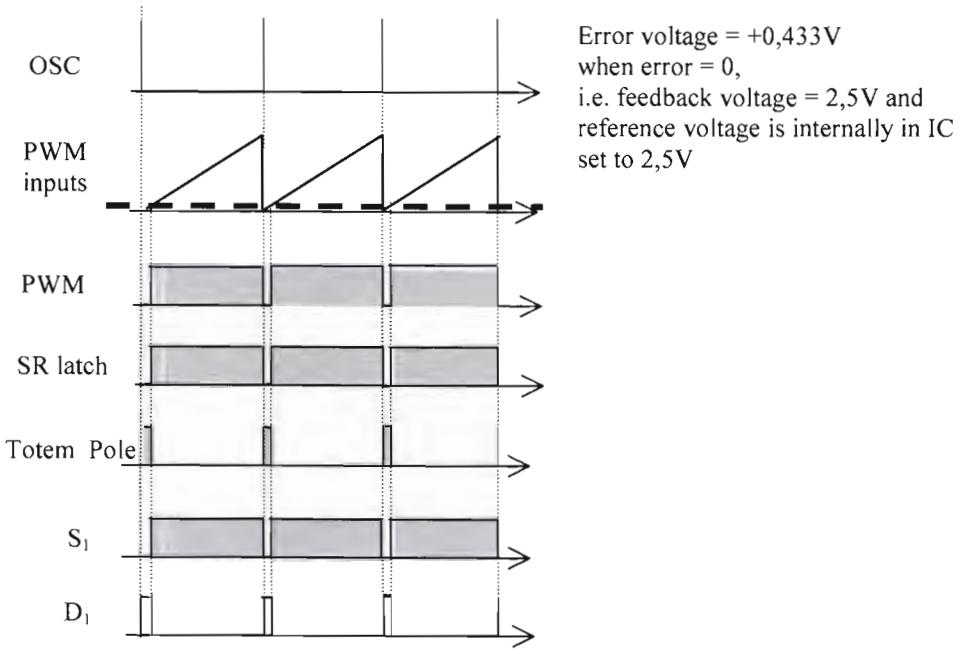


Figure 13: PWM action with error voltage about zero

2.2.1 Choice of frequency of operation

The frequency of operation should be such that it is at least ten times that of the fundamental frequency of the rectifier output. Since this is 100 Hz (twice the frequency of the mains supply of 50 Hz) an oscillator frequency of about 1000 Hz to 2000 Hz was deemed sufficient. The choice of frequency is dependant on the following criteria:

- Noise pollution
- Switching losses in the semiconductor devices
- Magnitude of the reactive components

For silent operation, the choice of frequency is above 20 kHz since the human ear responds only to frequencies below 20 kHz. However, the electronics in this case will be situated on a four meter pole located far from any dwelling and as such would not contribute to noise pollution since the sound level expected would be very low.
If the period is too long, the ability of the controller to respond adequately to a

change in the input current or output voltage is reduced. Thus the frequency of operation should first satisfy the control demand before the switching losses of the devices are considered.

The output capacitor size is inversely proportional to the switching frequency since the shorter the time that the capacitor has to sustain the supply current, the smaller will the change in capacitor voltage be. Mathematically, this can be expressed as follows:

From the basic equation for the charge relationship of a capacitor

$$Q = C\Delta V = I\Delta t \tag{8}$$

it follows that

$$\Delta V = \frac{I}{C}\Delta t \tag{9}$$

The inverter load should be about 2 kW. This would mean the load current would be

$$I_L = \frac{P}{V_L} = \frac{2000}{220} = 9,091 \text{ A} \tag{10}$$

Taking the oscillator frequency as 1000 Hz the period of the controller would be

$$t_p = \frac{1}{f} = \frac{1}{1000} = 1 \text{ ms} \tag{11}$$

Assuming a secondary current of 10 A from the CT, this would translate to a 14,14 A peak sinusoid. This means the current would be below 9,091 A for the first and last part of a half sinusoid given by

$$i = I_m \sin \omega t \tag{12}$$

$$9,091 = 14,14 \sin \omega t \tag{13}$$

$$\omega t = \sin^{-1}(\frac{9,091}{14,14}) \tag{14}$$

$$\omega t = 0.698 \tag{15}$$

$$t = \frac{0.698}{100\pi} \tag{16}$$

$$t = 2 \text{ ms} \tag{17}$$

Thus, the capacitor should be able to supply the load current on a cycle-to-cycle basis for double this period.

From equation (8) allowing the capacitor voltage to drop 10 V over the period of 4 ms, the capacitor value is:

$$C = \frac{I_L}{\Delta V}\Delta t = \frac{9,091}{10}(4 \times 10^{-3}) = 4000 \text{ µF} \tag{18}$$

In the case of a single-phase load, the inverter can be synchronized to the CT current zero crossings, which would minimize the load on the capacitor during the periods when the supply current falls to low levels. Taking a worst-case scenario, this means that a capacitor that only has to supply the load current for 1 ms should be sufficient. This would be a 1000 µF capacitor. From all of the above reasoning, a frequency choice of 1 to 2 kHz yields results that are acceptable all round.

Referring to Figure 14, the onboard oscillator operates as follows: C_T is charged via R_T from the internally derived 5 V reference source. (This provides an oscillator frequency that is insensitive to supply voltage variations.) When a predetermined

voltage level is reached, C_T is discharged via a constant current source. Thus the size of C_T will determine the dead-time of the IC output. Dead-time is the time that the IC output will be low. From the graph Dead-time vs. C_T (Figure 16) (Unitrode 1999:3-57), the dead time for a capacitor of 100 nF will be about 30 μs. The capacitor C_a in Figure 14 (Unitrode 1999:3-61) is a ceramic bypass capacitor of 0,1 μF that provides a path for high frequency transients that reach the output of V_{REF}. These transients are a result of the high current switching taking place in the circuit.

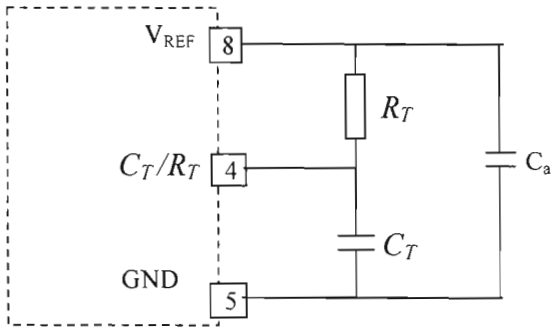


Figure 14: Timing components for the UC3842

The selection of oscillator frequency can be done by either choosing a timing capacitor C_T and then using the nomograph (Figure 15) to select the timing resistance R_T according to the desired frequency, or by using the formula in equation (19) to determine the components (Unitrode 1999:3-57).

$$F_{OSC} = \frac{1,72}{R_T C_T} = \frac{1,72}{(10k\Omega)(100nF)} = 1720 \text{ Hz} \qquad (19)$$

A 100 nF capacitor and a 10 kΩ resistor gives an oscillator frequency of 1720 Hz. However, the nature of the current source, as previously explained, necessitates a shunt operation of the main switch. This means that the dead-time mentioned for the IC will be the minimum closure-time for the switch.

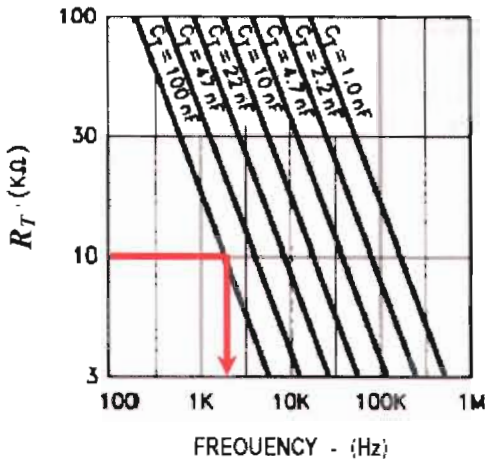


Figure 15: C_T R_T nomograph

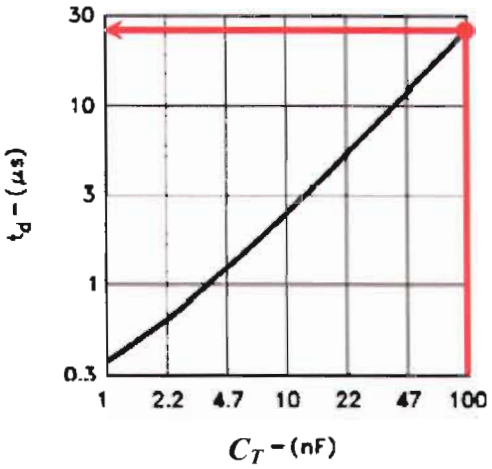


Figure 16: Dead-time versus C_T

The minimum % duty-cycle of the switch will thus be

$$D_{\min} = \frac{t_d}{t_p} \times 100 = \frac{30 \times 10^{-6}}{1 \times 10^{-3}} \times 100 = 3\ \% \tag{20}$$

and the maximum duty cycle will be 100 % . This is exactly what is required since the CT output must be shorted when a no-load condition is experienced.

2.2.2 PI controller transfer function

The transfer function of the basic active circuit in Figure 17 is given by

$$G_1(s) = \frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)} \tag{21}$$

(Nise 2000:66).

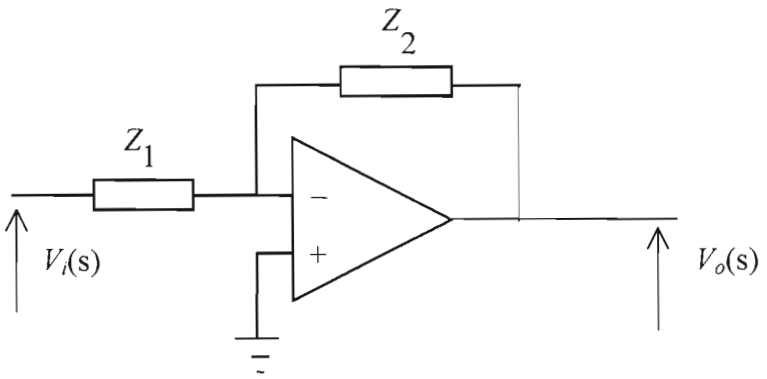


Figure 17: Basic active circuit

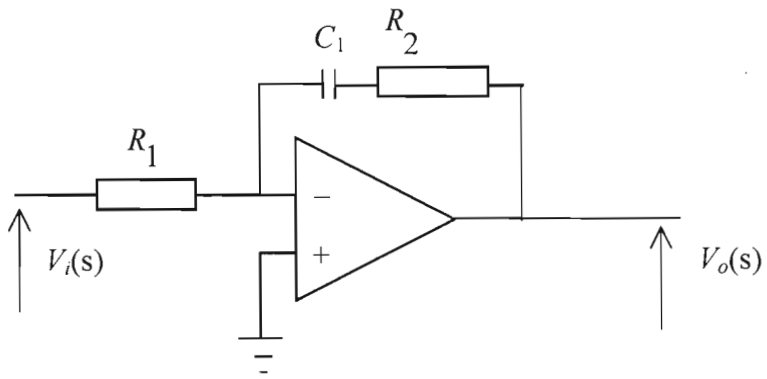


Figure 18: PI controller

For a simple PI controller (Figure 18):

$$Z_1(s) = R_1 \tag{22}$$

and

$$Z_2(s) = R_2 + \frac{1}{C_1 s} \tag{23}$$

Substituting equations (22) and (23) into (21) yields

$$G_1(s) = -\frac{R_2 + \frac{1}{C_1 s}}{R_1} \tag{24}$$

$$G_1(s) = -\left[\frac{R_2}{R_1} + \frac{1}{R_1 C_1 s}\right] \tag{25}$$

$$G_1(s) = -\frac{R_2}{R_1}\left[1 + \frac{1}{R_2 C_1 s}\right] \tag{26}$$

$$G_1(s) = -\frac{R_2}{R_1}\left[\frac{R_2 C_1 s + 1}{R_2 C_1 s}\right] \tag{27}$$

$$G_1(s) = -\frac{R_2}{R_1}\left[\frac{s + \frac{1}{R_2 C_1}}{s}\right] \tag{28}$$

$$G_1(s) = K\left[\frac{s + z_c}{s}\right] \tag{29}$$

where

$$K = -\frac{R_2}{R_1} \tag{30}$$

and

$$z_c = \frac{1}{R_2 C_1} \tag{31}$$

2.2.3 The feedback network transfer function

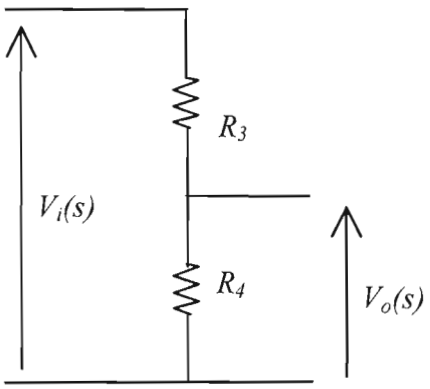


Figure 19: Feedback network

The feedback network transfer function is given by:

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_4}{R_3 + R_4} \tag{32}$$

$$H(s) = K_f \tag{33}$$

where

$$K_f = \frac{R_4}{R_3 + R_4} \tag{34}$$

2.2.4 The PWM transfer function

Referring to Figure 20, when the error voltage $v_e = 0$, the duty cycle should be zero. This means that there is no error. The voltage at the inverting input of the comparator ($v_{control}$) will then be:

$$v_{control} = (v_e - 2V_D)\left(\frac{R_a}{3R_a}\right) \tag{35}$$

Since the error amplifier (compensator) has an internal reference set to +2,5 volt, it implies that

$$v_e = 2,5 \text{ V} \tag{36}$$

when there is equilibrium in the circuit.

By substituting equation (36) into (35) the minimum value for the control voltage is:

$$v_{control_{min}} = (2,5 - 2(0,6))\left(\frac{1}{3}\right) = 0,433 \text{ V} \tag{37}$$

The manufacturer has set the upper limit of the control voltage to 1 volt. Therefore

$$v_{control_{max}} = 1 \text{ V} \tag{38}$$

Thus $v_{control_{max}}$ means a one hundred percent duty cycle and $v_{control_{min}}$ a three percent duty cycle as previously shown during the selection of the components for the fixed

frequency of the IC.

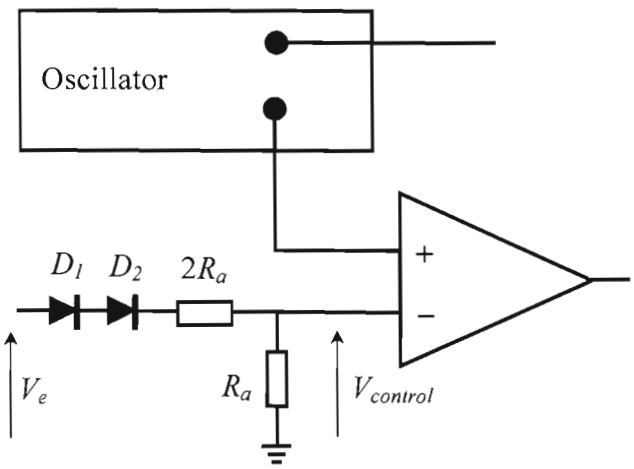


Figure 20: The pulse width modulator circuit

The transfer function of the PWM controller is given by:

$$G_2(s) = \frac{\text{change in duty cycle}}{\text{change in } v_{control}} \tag{39}$$

The above reasoning, as well as the substitution of equations (37) and (38) into (39) gives:

$$G_2(s) = \frac{100\text{-}3}{1-0,433} = 1,6755 \tag{40}$$

Let

$$G_2(s) = K_p \tag{41}$$

then

$$K_p = 1,6755 \tag{42}$$

Expressed in dB:

$$G_2(s) = 20\log(1,6755) \tag{43}$$

$$G_2(s) = 4,483 \text{ dB} \tag{44}$$

As can be seen, the transfer function of a pulse width modulator comes down to a gain.

2.2.5 The transfer function of the power stage including the capacitor

The feedback control system, of a direct duty ratio pulse width modulator used as a voltage regulator, can be illustrated by the block diagram in Figure 21 (Mohan 2003:323).

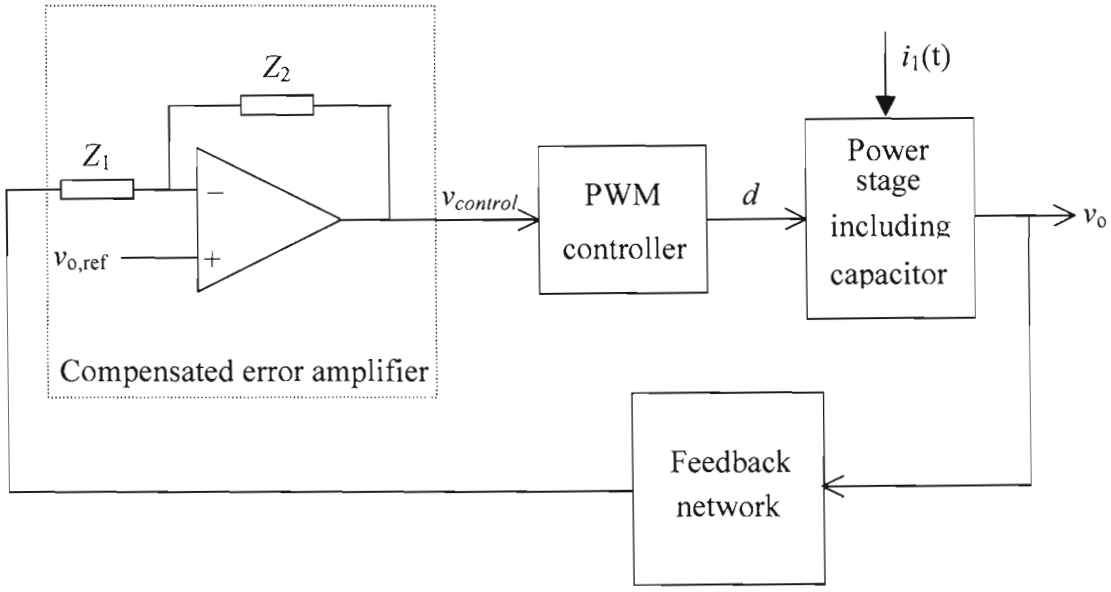


Figure 21: Feedback control system of the PWM voltage regulator

The linearized feedback control system is shown in Figure 22. The small AC signals are represented by "^". Since the transfer function of the compensated error amplifier as well as that of the pulse width modulator and feedback system have already been derived, all that is left regarding the block diagram in Figure 22 is that of the power stage which includes the capacitor as the plant.

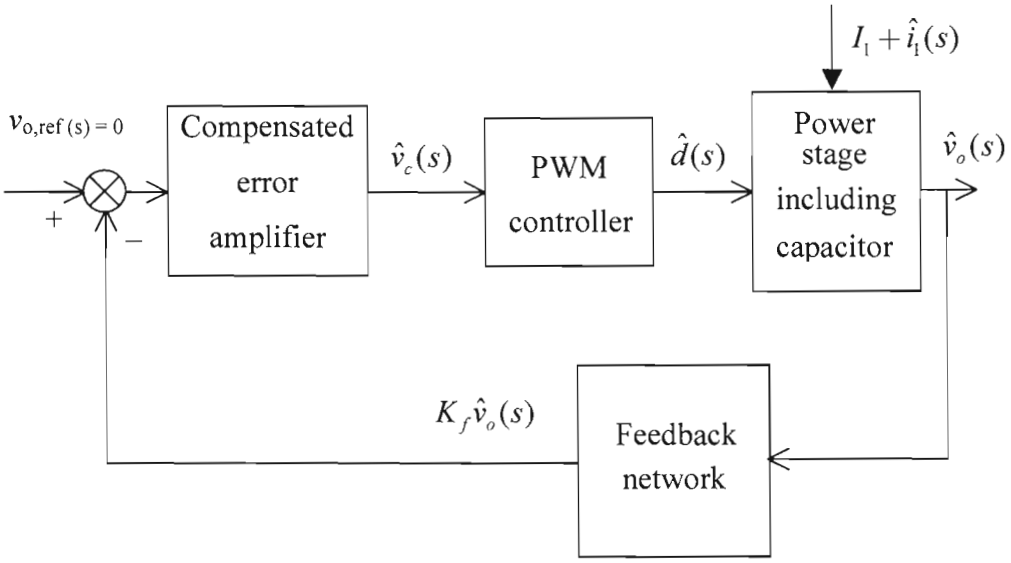


Figure 22: Linearized feedback control system

The state-space equations for the two possible circuit connections have to be written into the standard form shown in equations (45) and (46) (Erickson 2001:216).

$$\mathbf{K}\frac{\mathrm{dx(t)}}{\mathrm{dt}} = \mathbf{Ax(t)} + \mathbf{Bu(t)} \tag{45}$$

$$y(t) = \mathbf{C}x(t) + \mathbf{E}u(t) \tag{46}$$

Referring to Figure 23 and looking at the only storage element in the circuit, the *v-i* relation for the capacitor *C* is given by:

$$C\frac{dv_c(t)}{dt} = i_c(t) \tag{47}$$

Relating Figure 23 to equation (45), the state-vector $x(t)$ is $v_c(t)$, the input vector $u(t)$ is $i_1(t)$ and the output vector $y(t)$ is $v_o(t)$.

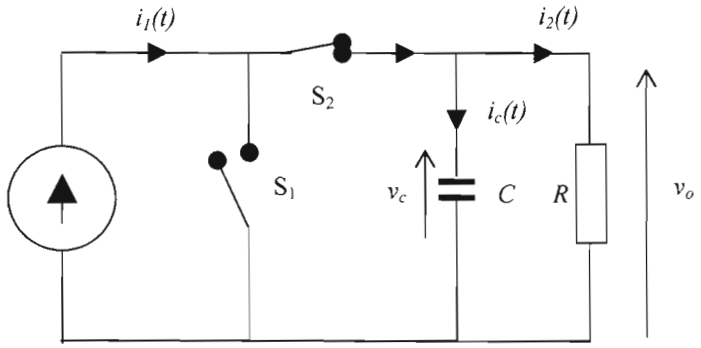


Figure 23: Simplified circuit for analysis

Two circuit states exist in the simplified circuit:

- State 1: S_1 closed, S_2 open
- State 2: S_1 open, S_2 closed

Applying KCL to the capacitor current during state 1:

$$i_c(t) = i_1(t) - i_2(t) \tag{48}$$

But

$$i_2(t) = \frac{v_c(t)}{R} \tag{49}$$

Substituting equation (49) into (48) yields:

$$i_c(t) = i_1(t) - \frac{v_c(t)}{R} \tag{50}$$

Substituting equation (50) into (47) yields:

$$C\frac{dv_c(t)}{dt} = i_1(t) - \frac{v_c(t)}{R} \tag{51}$$

$$C\dot{v}_c = i_1(t) - \frac{v_c(t)}{R} \tag{52}$$

where

$$\dot{v}_c = \frac{dv_c(t)}{dt} \tag{53}$$

The output voltage is given by:

$$v_o(t) = 0 + v_c(t) \tag{54}$$

During state 2 the equations are written as follows:

$$C\frac{dv_c(t)}{dt} = i_c(t) \tag{55}$$

where

$$i_c(t) = -\frac{v_c(t)}{R} \tag{56}$$

Substituting equation (56) into (55) yields:

$$C\frac{dv_c(t)}{dt} = -\frac{v_c(t)}{R} \tag{57}$$

$$C\dot{v}_c = -\frac{v_c(t)}{R} \tag{58}$$

The output voltage during state 2 is given by:

$$v_o(t) = 0 + v_c(t) \tag{59}$$

From equations (51) and (54) the matrix form of the state equations for state 1 can be written:

$$\mathbf{K}\frac{dx(t)}{dt} = \mathbf{A}_1 x(t) + \mathbf{B}_1 u(t) \tag{60}$$

$$[C]\frac{d}{dt}[v_c(t)] = \left[-\frac{1}{R}\right][v_c(t)] + [1][i_1(t)] \tag{61}$$

and

$$y(t) = \mathbf{C}_1 x(t) + \mathbf{E}_1 u(t) \tag{62}$$

$$v_o(t) = [1][v_c(t)] + [0][i_1(t)] \tag{63}$$

Similarly, using equations (57) and (59) the matrix form of the state equations for state 2 can be written:

$$\mathbf{K}\frac{dx(t)}{dt} = \mathbf{A}_2 x(t) + \mathbf{B}_2 u(t) \tag{64}$$

$$[C]\frac{d}{dt}[v_c(t)] = \left[-\frac{1}{R}\right][v_c(t)] + [0][i_1(t)] \tag{65}$$

and

$$y(t) = \mathbf{C}_2 x(t) + \mathbf{E}_2 u(t) \tag{66}$$

$$v_o(t) = [1][v_c(t)] + [0][i_1(t)] \tag{67}$$

The state-space averaged model describing the converter in equilibrium is given in equations (68) and (69):

$$0 = \mathbf{AX} + \mathbf{BU} \tag{68}$$

$$\mathbf{Y} = \mathbf{CX} + \mathbf{EU} \tag{69}$$

where

$\mathbf{X}$ = equilibrium (DC) state vector
$\mathbf{U}$ = equilibrium (DC) input vector
$\mathbf{Y}$ = equilibrium (DC) output vector

and the averaged matrices are

$$\mathbf{A} = D\mathbf{A}_1 + D'\mathbf{A}_2 \tag{70}$$

$$\mathbf{B} = D\mathbf{B}_1 + D'\mathbf{B}_2 \tag{71}$$

$$\mathbf{C} = D\mathbf{C}_1 + D'\mathbf{C}_2 \tag{72}$$

$$\mathbf{E} = D\mathbf{E}_1 + D'\mathbf{E}_2 \tag{73}$$

where

D = equilibrium (DC) duty cycle and

$$D' = (1\text{-}D) \tag{74}$$

(Erickson 2001:217)

Equations (68) and (69) can be used to solve for the equilibrium state and output vectors:

$$\mathbf{X} = \text{-}\mathbf{A}^{-1}\mathbf{B}\mathbf{U} \tag{75}$$

$$\mathbf{Y} = \left(-\mathbf{C}\mathbf{A}^{-1}\mathbf{B} + \mathbf{E}\right)\mathbf{U} \tag{76}$$

(Erickson 2001:217)

The state equations of the small signal AC model are given by the equations (77) and (78).

$$\mathbf{K}\frac{d\hat{x}(t)}{dt} = \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\mathbf{u}}(t) + \left[\left(\mathbf{A}_1 - \mathbf{A}_2\right)\mathbf{X} + \left(\mathbf{B}_1 - \mathbf{B}_2\right)\mathbf{U}\right]\hat{d}(t) \tag{77}$$

$$\hat{y}(t) = \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{E}\hat{\mathbf{u}}(t) + \left[\left(\mathbf{C}_1 - \mathbf{C}_2\right)\mathbf{X} + \left(\mathbf{E}_1 - \mathbf{E}_2\right)\mathbf{U}\right]\hat{d}(t) \tag{78}$$

Substituting from equations (61) and (65) into equation (70) to solve for **A**:

$$\mathbf{A} = D\left[-\frac{1}{R}\right] + D'\left[-\frac{1}{R}\right] \tag{79}$$

$$\mathbf{A} = \left(D + D^{'}\right)\left[-\frac{1}{R}\right] \tag{80}$$

but

$$\left(D + D^{'}\right) = 1 \tag{81}$$

Substituting equation (81) into (80) yields:

$$\mathbf{A} = \left[-\frac{1}{R}\right] \tag{82}$$

Substituting from equations (61) and (65) into equation (71) to solve for **B**:

$$\mathbf{B} = D[1] + D^{'}[0] \tag{83}$$

$$\mathbf{B} = [D] \tag{84}$$

Substituting from equations (63) and (67) into equation (72) to solve for **C**:

$$\mathbf{C} = D[1] + D^{'}[1] \tag{85}$$

$$\mathbf{C} = \left(D + D^{'}\right)[1] \tag{86}$$

$$\mathbf{C} = [1] \tag{87}$$

Substituting from equations (63) and (67) into equation (73) to solve for **E**:

$$\mathbf{E} = D[0] + D^{'}[0] \tag{88}$$

$$\mathbf{E} = [0] \tag{89}$$

From equation (77) the coefficient of $\hat{d}(t)$ is:

$$\left[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}\right] = \left[\left(-\frac{1}{R} - -\frac{1}{R}\right)V + (1-0)I\right] = I \tag{90}$$

where

V is the equilibrium (DC) voltage over the load and

I is the equilibrium (DC) input current

From equation (78) the coefficient of $\hat{d}(t)$ is:

$$\left[(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{E}_1 - \mathbf{E}_2)\mathbf{U}\right] = \left[(1-1)V + (0-0)I\right] = [0] \tag{91}$$

Substituting equations (82), (84), (87), (89), (90) and (91) into (77) and (78) yields the solved state equations of the small signal AC model:

$$C\frac{d\hat{v}_c(t)}{dt} = \left[-\frac{1}{R}\right]\hat{v}_c(t) + [D]\hat{i}_1(t) + I\hat{d}(t) \tag{92}$$

and

$$\hat{v}_o(t) = \hat{v}_c(t) \tag{93}$$

Equations (92) and (93) have been used to sketch the small signal AC equivalent circuit in Figure 24.

Substituting equation (93) into (92) yields

$$C\frac{d\hat{v}_o(t)}{dt}=\left[-\frac{1}{R}\right]\hat{v}_o(t)+[D]\hat{i}_1(t)+I\hat{d}(t) \tag{94}$$

Ignoring any variation in $i_1(t)$ and converting to the s-domain:

$$Cs\hat{v}_o(s)=-\frac{1}{R}\hat{v}_o(s)+I\hat{d}(s) \tag{95}$$

$$\hat{v}_o(s)(1+sRC)=IR\hat{d}(s) \tag{96}$$

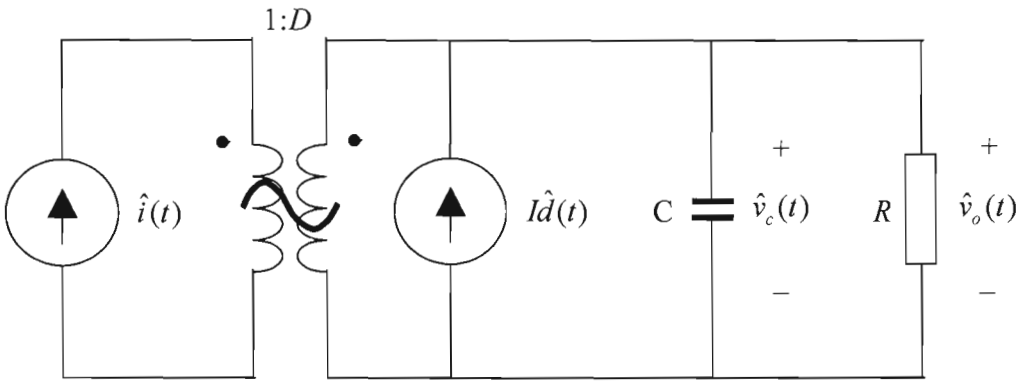


Figure 24: Small signal AC equivalent circuit of TRAFTAP1

$$\frac{\hat{v}_o(s)}{\hat{d}(s)}=\left[\frac{IR}{(1+sRC)}\right]\left(\frac{\frac{1}{RC}}{\frac{1}{RC}}\right) \tag{97}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)}=\frac{I}{C}\times\frac{1}{\left(s+\frac{1}{RC}\right)} \tag{98}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)}=\frac{I}{C}\times\frac{1}{(s+z_a)} \tag{99}$$

where

$$z_a = \frac{1}{RC} \tag{100}$$

Let

$$G_3(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} \tag{101}$$

then

$$G_3(s) = \frac{I}{C} \times \frac{1}{(s + z_a)} \tag{102}$$

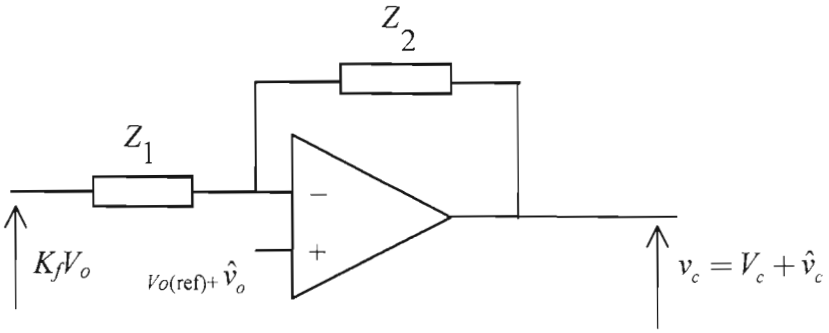


Figure 25: A general compensated error amplifier

2.2.6 Application of the PI controller in a direct duty ratio PWM

Comparing Figure 21 with Figure 18 reveals that the non-inverting input of the PI opamp circuit is connected to ground, while in the direct duty ratio pulse-width modulator, the reference input is connected to the non-inverting input of the opamp. From the linearized feedback control system in Figure 22 a general compensated error amplifier can be sketched as shown in Figure 25. The AC small signal transfer

function can be seen to be

$$\frac{\hat{v}_c}{\hat{v}_o} = 1 + \frac{Z_2}{Z_1} \tag{103}$$

since the variation will be applied to the non-inverting input and will have the transfer function of a non-inverting amplifier.

However, for all practical considerations, the ratio of

$$\frac{Z_2}{Z_1} >> 1 \tag{104}$$

Therefore

$$\frac{\hat{v}_c}{\hat{v}_o} \approx \frac{Z_2}{Z_1} \tag{105}$$

Thus the transfer function of the PI controller given in equation (28) changes to:

$$G_1(s) = \frac{R_2}{R_1}\left[\frac{s + \frac{1}{R_2 C_1}}{s}\right] \tag{106}$$

$$G_1(s) = K_1\left[\frac{s + \frac{1}{R_2 C_1}}{s}\right] \tag{107}$$

where

$$K_1 = \frac{R_2}{R_1} \tag{108}$$

2.2.6 The open loop transfer function

The open loop transfer function is given by

$$L(s) = G(s)H(s) \tag{109}$$

where

$$G(s) = G_1(s)G_2(s)G_3(s) \tag{110}$$

Substituting equations (41), (102) and (106) into (110) yields

$$G(s) = K_1\left(\frac{s+z_c}{s}\right) \times K_p \times \left(\frac{I}{C} \times \frac{1}{s+z_a}\right) \tag{111}$$

$$G(s) = \frac{IK_1K_p}{C}\left(\frac{s+z_c}{s^2+z_a s}\right) \tag{112}$$

Substituting equations (112) and (33) into (109) yields

$$L(s) = \frac{IK_1K_fK_p}{C}\left(\frac{s+z_c}{s^2+z_a s}\right) \tag{113}$$

2.2.7 Reducing the subsystems to one transfer function

The block diagram of the subsystem is shown in Figure 26. This block diagram can be reduced into a single block representing the transfer function from input to output

(Nise 2000:256). From this equivalent transfer function the percentage overshoot, settling time, peak time and rise time can be found (Nise 2000:261).

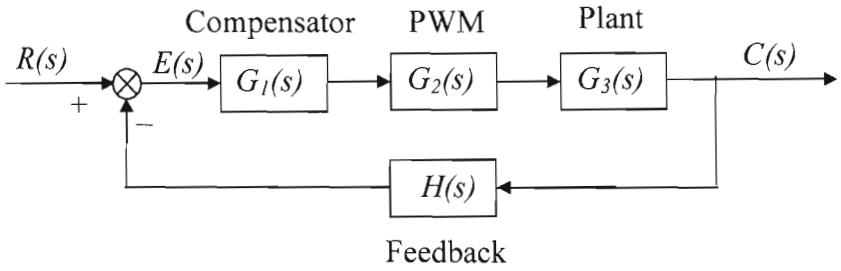


Figure 26: Subsystem block diagram

Referring to Figure 26, the closed loop transfer function of the system is given by

$$T(s)=\frac{C(s)}{R(s)} \tag{114}$$

where

$$C(s)=G_1(s)G_2(s)G_3(s) \tag{115}$$

and

$$R(s)=1+G_1(s)G_2(s)G_3(s)H(s) \tag{116}$$

Substituting equations (115) and (116) into (114) yields the equivalent transfer function of the controller:

$$T(s)=\frac{G_1(s)G_2(s)G_3(s)}{1+G_1(s)G_2(s)G_3(s)H(s)} \tag{117}$$

Substituting equations (33), (41), (102) and (107) into (117) yields

$$T(s)=\frac{\frac{IK_1K_p}{C}\left(\frac{s+z_c}{s^2+z_as}\right)}{1+\frac{IK_1K_pK_f}{C}\left(\frac{s+z_c}{s^2+z_as}\right)} \tag{118}$$

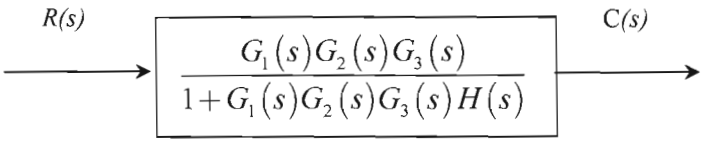


Figure 27: Reduction to a single block

Let

$$\beta=\frac{IK_1K_pK_f}{C} \tag{119}$$

Substitute equation (119) into (118):

$$T(s)=\frac{\frac{\beta}{K_f}\left(\frac{s+z_c}{s^2+z_as}\right)}{1+\beta\left(\frac{s+z_c}{s^2+z_as}\right)} \tag{120}$$

$$T(s)=\frac{\frac{\beta}{K_f}\left(\frac{s+z_c}{s^2+z_as}\right)}{\left(\frac{s^2+z_as+\beta(s+z_c)}{(s^2+z_as)}\right)} \tag{121}$$

$$T(s)=\frac{\dfrac{\beta}{K_f}\left(\dfrac{s+z_c}{s^2+z_a s}\right)}{\left(\dfrac{s^2+(z_a+\beta)s+\beta z_c}{(s^2+z_a s)}\right)} \tag{122}$$

$$T(s)=\frac{\beta}{K_f}\left(\frac{s+z_c}{s^2+z_a s}\right)\times\left(\frac{(s^2+z_a s)}{s^2+(z_a+\beta)s+\beta z_c}\right) \tag{123}$$

$$T(s)=\left(\frac{\dfrac{\beta}{K_f}(s+z_c)}{s^2+(z_a+\beta)s+\beta z_c}\right) \tag{124}$$

Let

$$\omega_n^2=\beta z_c \tag{125}$$

and

$$2\zeta\omega_n=z_a+\beta \tag{126}$$

where

ζ is the damping ratio and

ω_n is the natural undamped frequency.

Substituting equations (125) and (126) into (124) yields:

$$T(s)=\frac{1}{z_c K_f}\left(\frac{\omega_n^2(s+z_c)}{s^2+2\zeta\omega_n s+\omega_n^2}\right) \tag{127}$$

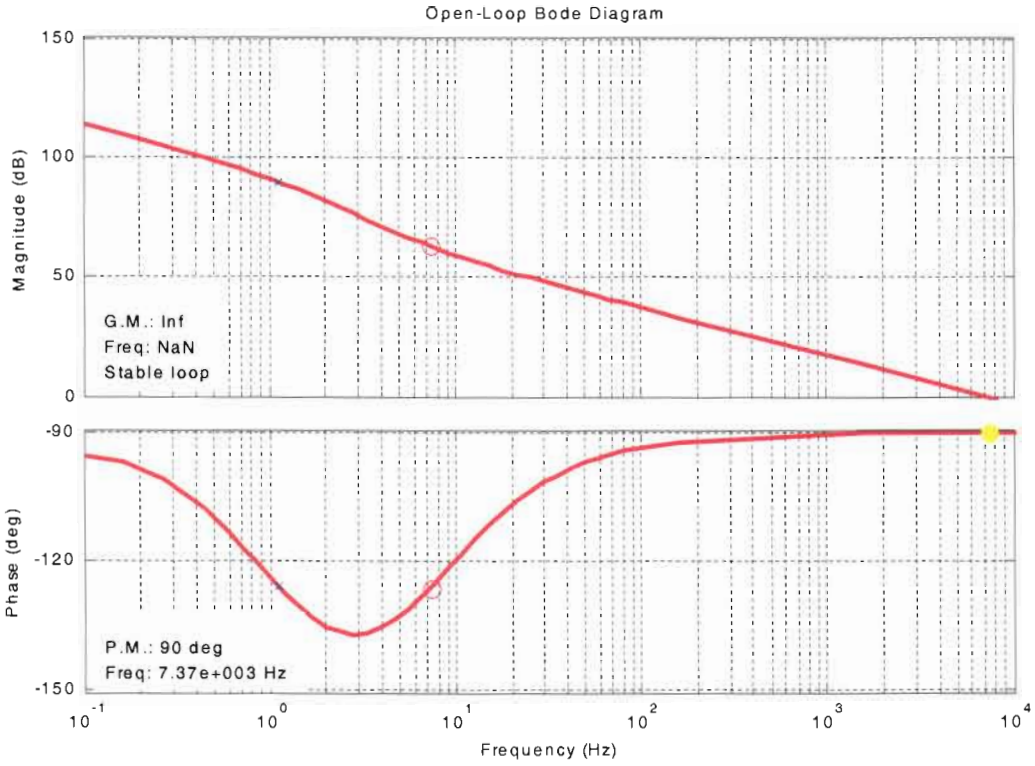


Figure 28: Open-loop Bode diagram of system

From equations (125) and (126) the damping ratio and natural undamped frequency can be found:

$$\omega_n = \sqrt{\beta z_c} \tag{128}$$

$$\zeta = \frac{z_a + \beta}{2\omega_n} \tag{129}$$

2.2.8 Evaluating the system for stability

The transfer functions above were used in MATLAB to evaluate the response of the system in order to determine whether the system is stable or not. A screen snapshot

of the program to transfer all of the transfer functions into the workspace of MATLAB is shown in Annexure A.

Figure 28 shows the open-loop Bode diagram from which it can be seen that the phase margin is 90° and the gain margin is infinite. The system is therefore stable. The step response in Figure 29 shows that the system has a fast reaction time to any change in output voltage – the rise time being 83,7 μs. No overshoot and no oscillations are observed. The open-loop Nichols chart in Figure 30 also shows that the system is stable. The Nyquist diagram shown in Figure 31 confirms the stability of the system.

2.2.9 Effect of saturation on the step response

In any PWM system, the natural limits to the duty cycle are 0% and 100%. A switch cannot be ON for longer than the repetition period. Neither can it be ON for less than zero seconds. This translates to a saturation effect in a control system. Although the control signal can indicate that a greater than 100% pulse width is required, in a practical circuit the switch will just be ON for the complete period, the period being fixed. In order to compare the results that were obtained during simulations, a saturation block was inserted into the block diagram of the system as shown in Figure 29. The step response of the system was evaluated with saturation. The step response is shown in Figure 32. It shows no overshoot, ringing or instabilities.

2.3 Summary

The principle of duality lends itself excellently as an aid in understanding the way in which the current transformer is used in this application. A block diagram of the TRAFTAP1 system was presented. It was noted that the CT in this system is a transformer intended to provide power and therefore not the same as a measurement or protection CT. Such a high voltage transformer does not yet exist (2005) and will

still have to be designed. A protection circuit to protect the CT against over voltages in the case of a failure of the electronics coupled to the CT is needed. To this end an AC crowbar design was proposed and discussed. This was followed by an explanation of the basic current source to voltage source converter circuit. Adding the relevant circuit from a controller IC, the complete action of the circuit was analysed and explained. Certain aspects of the design and analysis of the PI controller were expounded. These included:

- the choice of operational frequency,
- transfer functions of the blocks forming the closed loop PI controller,
- derivation of the small signal AC equivalent circuit by using averaging and linearization state space techniques as well as
- the need for including a non-linear saturation block in the system block diagram.

Utilizing MATLAB, the stability of the design was shown with a Bode diagram, Nyquist diagram, Nichols chart as well as a step response. This was all done according to the classical control approach. The step response after introducing the non-linear saturation block concluded this chapter. In the next chapter, the theory of the TRAFTAP2 system will be presented.

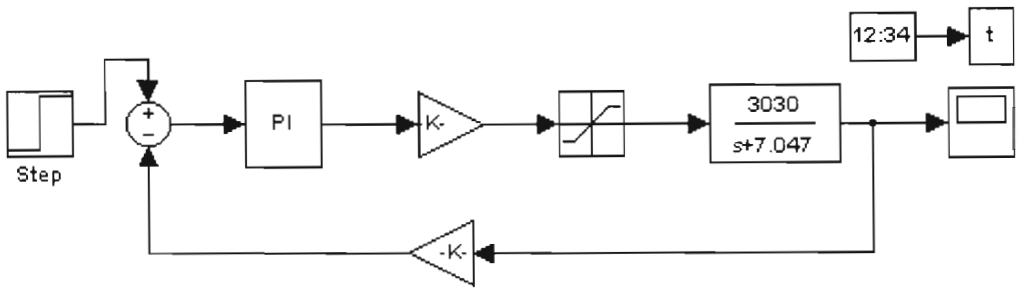


Figure 29: Saturation included in system block diagram using Simulink

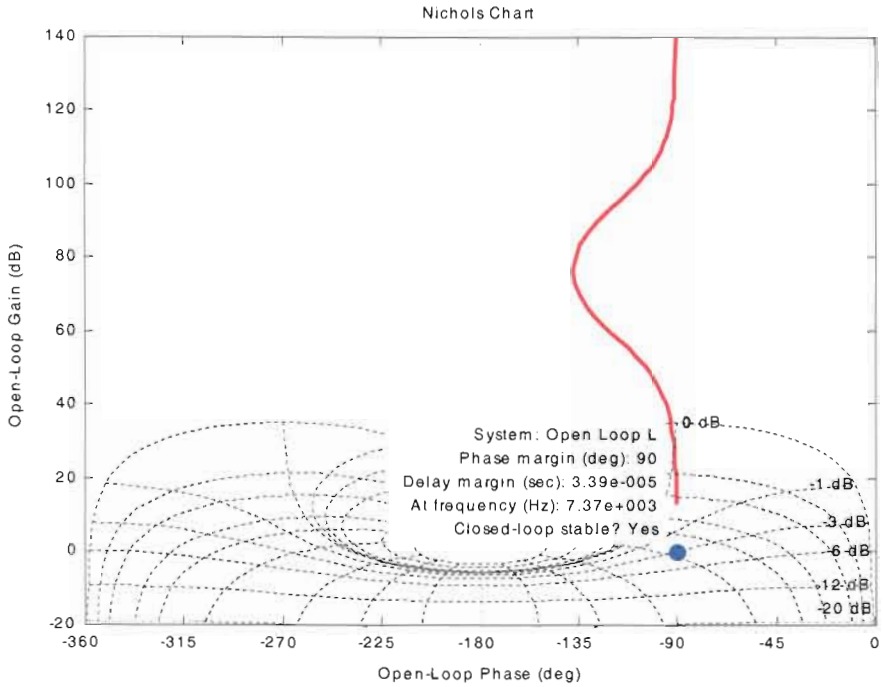


Figure 30: Open loop Nichols chart of the system

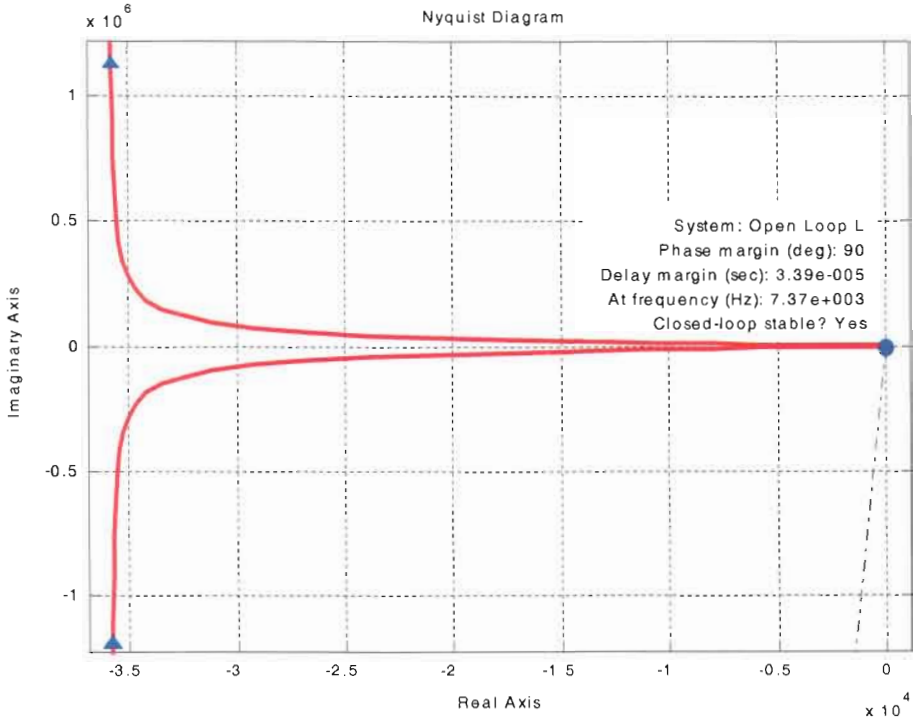


Figure 31: Nyquist diagram of the system

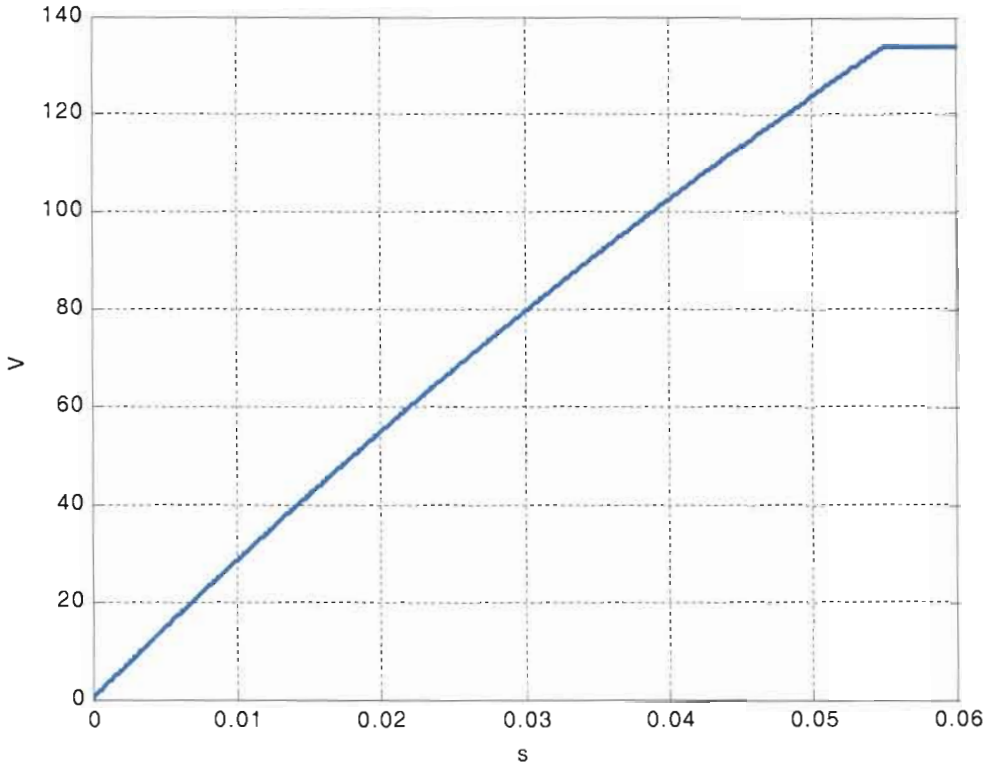


Figure 32: Step response with saturation

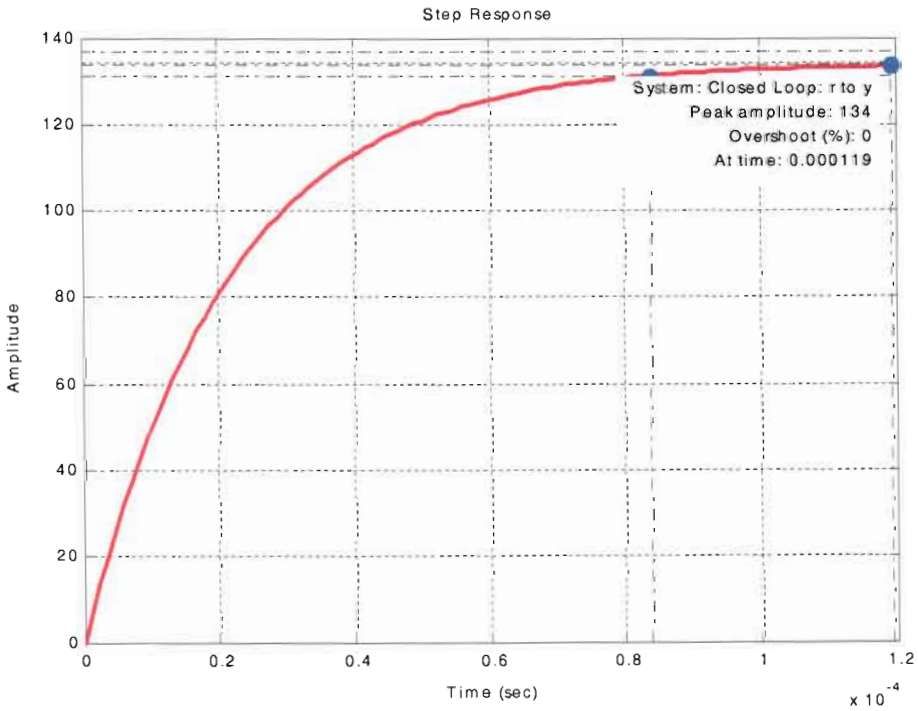


Figure 33: Step response of the system

Chapter 3 Direct alternating current to alternating voltage conversion

The possibility of controlling the output voltage of a current transformer via an additional test-winding can be hypothesized by examining the statement made by Jenkins (1967:110) with reference to a test-winding on a current transformer: "... if the primary winding is energized and the secondary winding is connected to its burden, then a short-circuited test-winding on the same core would mean a complete breakdown of the normal relationship between the primary current and the secondary current; the current flowing through the burden in this condition would not be that given by the nominal ratio of the current-transformer". The proposed solution is shown in Figure 34.

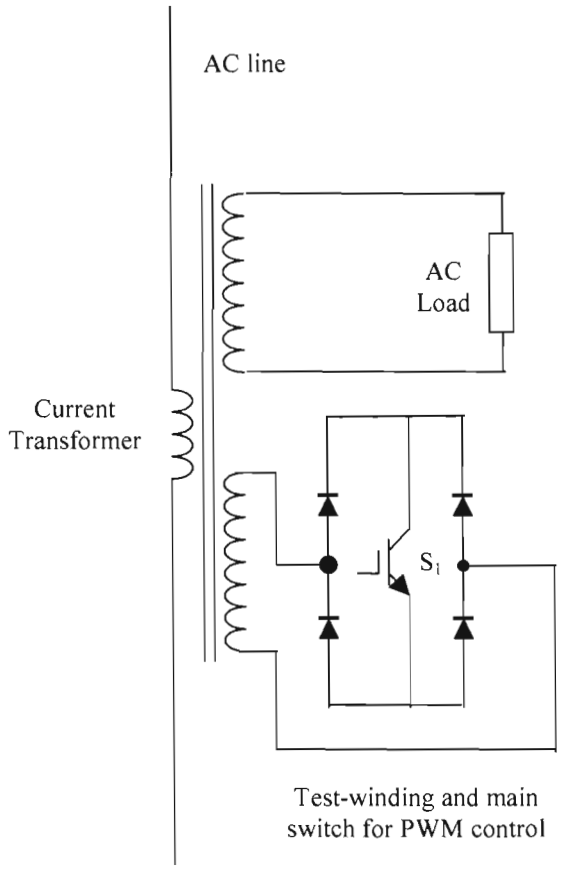


Figure 34: Current to voltage conversion with PWM control via "test winding"

3.1 Theory

There are two frequencies in this system. One is the utility supply frequency (50 Hz) and the other is the chopping/control frequency (f_c), which is much higher than the utility frequency.

The magnetic flux in the current transformer can be described as:

$$\Phi_p = \Phi_s + \Phi_c + \Phi_l \tag{130}$$

where:

Φ_p is the flux created by the primary current, i_p

Φ_s is the counter flux created by the current in the secondary winding,

Φ_c is the counter flux created by the current in the control winding and

Φ_l is the leakage flux .

The leakage flux is negligible due to the toroidal geometry of the magnetic core, thus:

$$\Phi_l = 0 \tag{131}$$

During the chopping period (T_c), the switch S_1 is closed for kT_c seconds (k being the duty cycle), the current in the control winding becomes maximum and the flux can be described by:

$$\Phi_c = \Phi_p \tag{132}$$

Substituting equations (131) and (132) into (130) gives

$$\Phi_s = 0 \tag{133}$$

When the switch S_1 is open, the current in the control winding is zero and the equations describing the flux become:

$$\Phi_c = 0 \tag{134}$$

and

$$\Phi_s = \Phi_p \tag{135}$$

The average flux in the secondary winding as seen from the utility frequency point of view is:

$$\tilde{\Phi}_s = \frac{1}{T_c}\int_0^{T_c} \Phi_s dt \tag{136}$$

$$\tilde{\Phi}_s = (1-k)\Phi_p \tag{137}$$

$$\tilde{\Phi}_s = k'\Phi_p \tag{138}$$

where

$$k' = (1-k) \tag{139}$$

According to Faraday's law:

$$v_s = \frac{d}{dt}\tilde{\Phi}_s \tag{140}$$

Thus

$$v_s = C \times k' \times i_p \tag{141}$$

where C is a constant depended on the geometry of the transformer and utility frequency.

From equation (141) the secondary load voltage v_s depends on the primary current and duty cycle. The secondary load voltage also has the same frequency as the primary current. This shows that there is a direct conversion from an alternating current source to an alternating voltage source with the possibility of controlling the output voltage via the duty cycle of the control winding.

Further more, by comparing the output voltage of the secondary winding to that of a sinusoidal reference voltage, an error voltage can be produced that can be used to pulse-width modulate a switch on a test winding (used as a control winding) in such a manner that the secondary voltage will be sinusoidal under a whole range of loads. This would mean that the chopping frequency would vary. Alternatively, the average output in the previous cycle can be used to determine the pulse-width of a current cycle. In this case the chopping frequency would be fixed (Mazda 1997:171, 172).

3.1.1 Equal time ratio control

The specific mode of control selected for the control of the AC chopper is "equal time ratio control" (ETRC), since it provides a linear relationship between the fundamental component and the control variable k'. This eases the control of the chopper considerably. Also, the more inductive the load, the nearer the rms value of the output current is to that of the fundamental. This is also dependent on the ratio between chopping frequency and that of the AC waveform. The greater the ratio, the better the waveform (Addoweesh 1993:1003 - 1007).

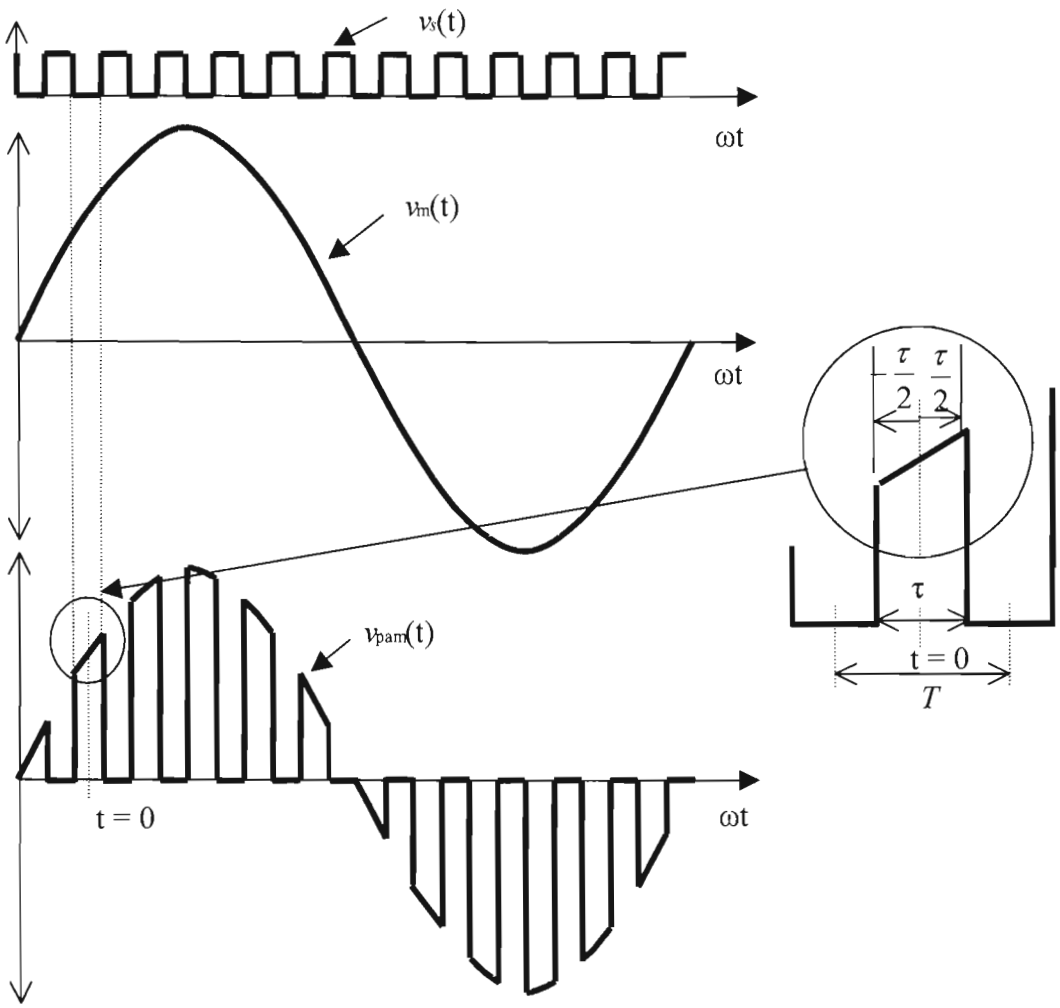


Figure 35: Illustration showing the generation of the ETRC output voltage

The input current in a voltage sourced AC chopper as presented by Addoweesh (1993) is not applicable to the proposed current sourced AC chopper, because the current will not be interrupted in the supply but will be simply shunted away from the load.

3.1.2 Mathematical derivation of output waveform

The output waveform can be seen to be the same as that of a train of pulse amplitude modulated (PAM) pulses. The mathematical expression for the output waveform can be obtained by

$$v_{PAM}(t) = v_m(t) \times v_s(t) \tag{142}$$

A single pulse is denoted by

$$p(t) = \begin{cases} E \text{ for } \frac{-\tau}{2} < t < \frac{\tau}{2} \\ 0 \text{ elsewhere} \end{cases} \tag{143}$$

and an infinite train of pulses with period T is represented by

$$P(t) = \sum_{n=1}^{\infty} p(t - nT) \tag{144}$$

(Marshall 1980:38).

A pulse train is periodic and can be represented by the general Fourier series:

$$v_s(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{n=1}^{\infty} b_n \sin n\omega t \tag{145}$$

where

$$a_0 = \frac{1}{T} \int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} f(t)dt \tag{146}$$

From the enlarged portion shown in Figure 35 the average term is:

$$\Rightarrow a_0 = \frac{1}{T} \int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} E dt \tag{147}$$

$$\Rightarrow a_0 = \frac{E}{T}[t]_{\frac{-\tau}{2}}^{\frac{\tau}{2}} = \frac{E\tau}{T} \tag{148}$$

Let time $t = 0$ be in the centre of each pulse, then in equation (145) all b_n coefficients are zero and the a_n coefficients are given by:

$$a_n = \frac{2}{T}\int_{\frac{-\tau}{2}}^{\frac{\tau}{2}} f(t)\cos n\omega t dt \tag{149}$$

$$= \frac{2}{T}\int_{\frac{-\tau}{2}}^{\frac{\tau}{2}} E\cos n\omega t dt \tag{150}$$

$$= \frac{2E}{T}\left[\frac{\sin n\omega t}{n\omega}\right]_{\frac{-\tau}{2}}^{\frac{\tau}{2}} \tag{151}$$

$$= \frac{2E}{n\omega T}\left[\sin\frac{n\omega\tau}{2} - \sin\frac{-n\omega\tau}{2}\right] \tag{152}$$

$$= \frac{4E}{\mathrm{n}\omega T}\sin\frac{n\omega\tau}{2} \tag{153}$$

$$= \frac{4E\tau}{\mathrm{n}\omega\tau T}\sin\frac{n\omega\tau}{2} \tag{154}$$

$$= \frac{2E\tau}{\frac{n\omega\tau}{2}T}\sin\frac{n\omega\tau}{2} \tag{155}$$

$$= \frac{2E\tau}{T} \frac{\sin \frac{n\omega\tau}{2}}{\frac{n\omega\tau}{2}} \tag{156}$$

Substituting equations (148) and (156) into (145) yields:

$$v_s(t) = \frac{E\tau}{T} + \frac{2E\tau}{T} \sum_{n=1}^{\infty} \frac{\sin \frac{n\omega\tau}{2}}{\frac{n\omega\tau}{2}} \times \cos n\omega t \tag{157}$$

(Conner 1972:16).

If E is normalized to 1 V peak and the sampling frequency is taken as f_s then the unmodulated pulse train is given by:

$$v_s(t) = \frac{\tau}{T} + \frac{2\tau}{T} \sum_{n=1}^{\infty} \frac{\sin \frac{n\omega_s\tau}{2}}{\frac{n\omega_s\tau}{2}} \times \cos n\omega_s t \tag{158}$$

(Conner 1973:50-52).

The modulating signal in the case of the TRAFTAP2 system is the output voltage of the CT, which is given by

$$v_m(t) = V_m \sin \omega_m t \tag{159}$$

Multiply equation (158) and (159) to obtain an expression for the modulated pulse train as in equation (142):

$$v_{PAM}(t) = v_m(t) \times v_s(t) \tag{160}$$

$$v_{PAM}(t) = (V_m \sin \omega_m t) \times \left[\frac{\tau}{T} + \frac{2\tau}{T} \sum_{n=1}^{\infty} \left(\frac{\sin \frac{n\omega_s \tau}{2}}{\frac{n\omega_s \tau}{2}} \times \cos n\omega_s t \right) \right] \tag{161}$$

Let the control variable

$$k' = \frac{\tau}{T} \tag{162}$$

Substitute equation (162) into (161)

$$v_{PAM}(t) = k'V_m \sin \omega_m t + 2k'V_m \sum_{n=1}^{\infty} \left[\frac{\sin \frac{n\omega_s \tau}{2}}{\frac{n\omega_s \tau}{2}} \times \cos n\omega_s t \times \sin \omega_m t \right] \tag{163}$$

But

$$\sin A \cos B = \frac{1}{2}\left(\sin(A+B) + \sin(A-B)\right) \tag{164}$$

Applying equation (164) to (163):

$$v_{PAM}(t) = k'V_m \sin \omega_m t + 2k'V_m \sum_{n=1}^{\infty} \left[\frac{\sin \frac{n\omega_s \tau}{2}}{\frac{n\omega_s \tau}{2}} \times \frac{1}{2}\left\{\sin(\omega_m + n\omega_s)t + \sin(\omega_m - n\omega_s)t\right\} \right] \tag{165}$$

$$= k'V_m \sin \omega_m t + k'V_m \sum_{n=1}^{\infty} \left[\frac{\sin \frac{n\omega_s \tau}{2}}{\frac{n\omega_s \tau}{2}} \times \left\{\sin(\omega_m + n\omega_s)t + \sin(\omega_m - n\omega_s)t\right\} \right] \tag{166}$$

$$= k'V_m \sin\omega_m t + k'V_m \sum_{n=1}^{\infty} \left[\frac{\sin \frac{n2\pi \frac{\tau}{T}}{2}}{\frac{n2\pi \frac{\tau}{T}}{2}} \times \left\{ \sin(\omega_m + n\omega_s)t + \sin(\omega_m - n\omega_s)t \right\} \right] \quad (167)$$

$$= k'V_m \sin\omega_m t + k'V_m \sum_{n=1}^{\infty} \left\{ \frac{\sin \pi n k'}{n k' \pi} \times \left[\sin(\omega_m + n\omega_s)t + \sin(\omega_m - n\omega_s)t \right] \right\} \quad (168)$$

$$= k'V_m \sin\omega_m t + \frac{k'V_m}{k'} \sum_{n=1}^{\infty} \left[\frac{\sin \pi n k'}{\pi n} \times \left\{ \sin(\omega_m + n\omega_s)t + \sin(\omega_m - n\omega_s)t \right\} \right] \quad (169)$$

$$= k'V_m \sin\omega_m t + V_m \sum_{n=1}^{\infty} \left[\frac{\sin nk'\pi}{\pi n} \times \left\{ \sin(\omega_m + n\omega_s)t + \sin(\omega_m - n\omega_s)t \right\} \right] \quad (170)$$

(Case 1980:123) (Addoweesh 1993:999-1013)

Equation (170) differs from that found in Mazda (1997:169), which erroneously has left out the constant π.

Traditionally, AC chopper regulators are primarily used where the load requires a sine wave, since the fundamental chopper frequency can easily be removed by a series band stop filter and a low pass filter can be used to remove the higher order harmonics (Mazda 1997:171).

3.2 Certain aspects of analysis and design

The ETRC was implemented with a PIC18F452 microcontroller. A digital PID controller was realized by using the program in Annexure B.

3.2.1 The PID controller

In the continuous time domain a PID algorithm has the following general form:

$$u(t) = K_p e(t) + \frac{K_p}{T_i}\int_0^t e(t)dt + K_p T_d \frac{de(t)}{dt} \tag{171}$$

where

$e(t)$ is the error signal,

$u(t)$ is the control input to the process,

K_p is the proportional gain,

T_i is the integral time constant and

T_d is the derivative time constant.

(Ibrahim 2002:185)

In the s-domain, equation (171) can be written as

$$U(s) = K_p\left(1 + \frac{1}{sT_i} + sT_d\right)E(s) \tag{172}$$

The z-transform of equation (172) will yield the discrete form of a PID controller:

$$U(z) = E(z)K_p\left[1 + \frac{T}{T_i\left(1-z^{-1}\right)} + T_d\frac{\left(1-z^{-1}\right)}{T}\right] \tag{173}$$

where T is the sampling interval.

Rewriting equation (173) as a transfer function yields:

$$\frac{U(z)}{E(z)} = a + \frac{b}{\left(1 - z^{-1}\right)} + c\left(1 - z^{-1}\right) \tag{174}$$

where

$$a = K_p,$$

$$b = \frac{K_p T}{T_i} \text{ and}$$

$$c = \frac{K_p T_d}{T}.$$

(Ibrahim 2002:194)

Equation (174) can be used to realize a parallel programming algorithm, which when implemented in a c-program will provide the necessary PID controller (Figure 36).

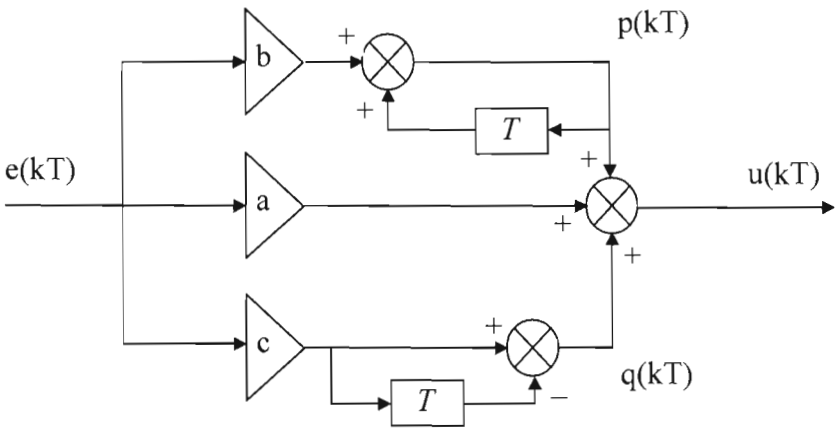


Figure 36: Parallel realization of the PID controller (Ibrahim 2002:195)

The c-program for the PID controller is listed in Annexure B. Since the response time needed is relatively slow, the Ziegler-Nichols settings (Ibrahim 2002:187) were used as a starting point and the values of T_i, T_d and K_p adjusted until a reasonable response was obtained. The values are to be found in the program listing in Annexure B.

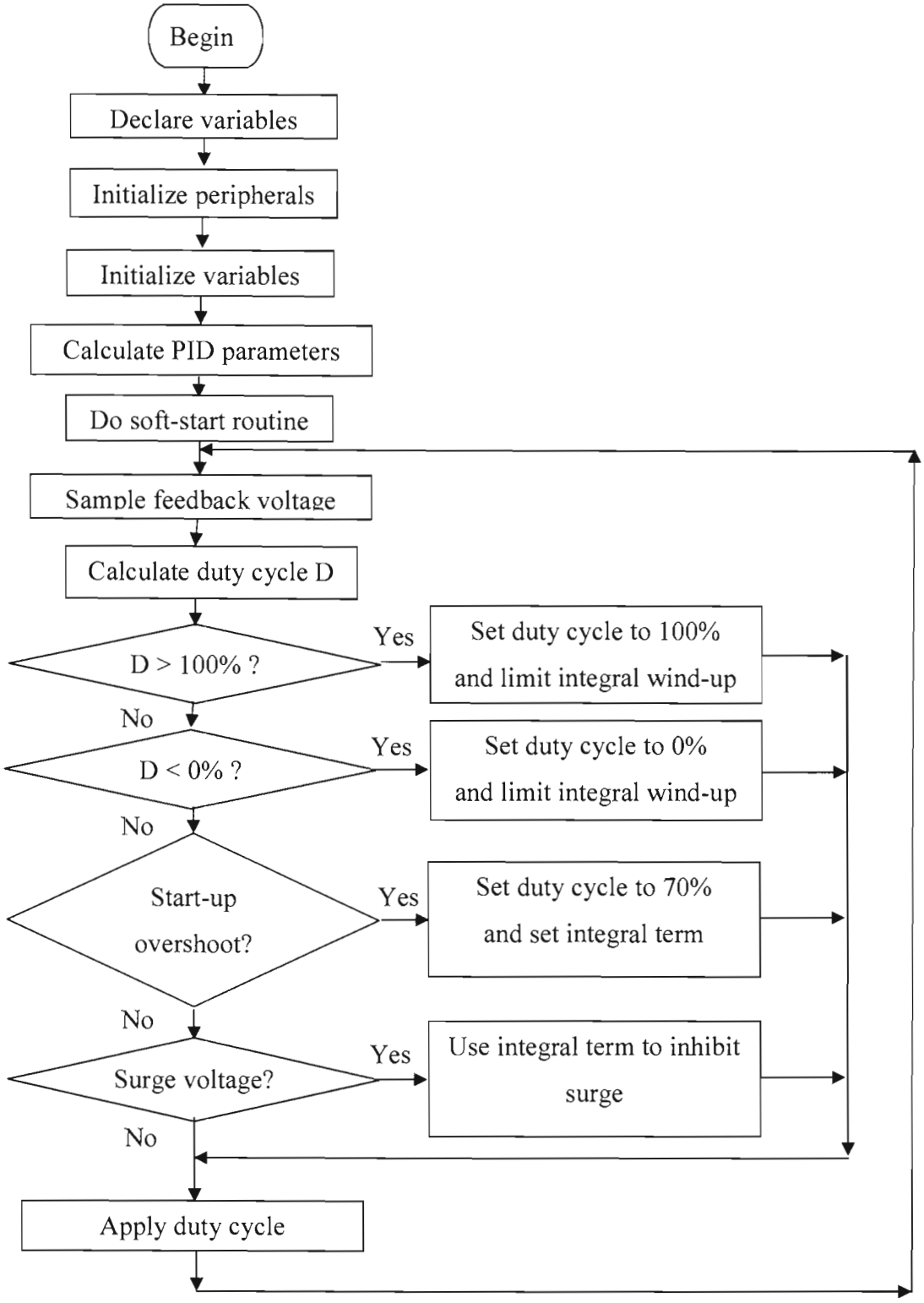


Figure 37: PID algorithm flowchart

Since over-voltage surges can be detrimental to the load, intelligence was included into the PID controller to restrict the load voltage by drastically reducing the output voltage for a few cycles in the event of a positive cycle exceeding a predetermined level (20%) above the nominal output voltage. This was done by making the integral term a large negative value, which although introducing a sudden reduction in the duty cycle and thus the output voltage, did not cause ringing and also allowed for a gradual return to the regulated output voltage required by the load.

3.3 The TRAFTAP2 CT

The CT must be designed with two secondary windings. In order to minimize the stress on the main switch, the control winding voltage must be kept low while the current will be high. Low voltage devices are currently capable of switching large currents and have a low on-state resistance (MOSFET's). The load winding should have a voltage rating that is higher than that required by the load since allowance must be made for the volt drop over the filter inductor. A power CT designer with a user-friendly interface was created in MS Excel. A screen snapshot of this tool is shown in Annexure C.

3.4 Summary

In this chapter the basic operation of the direct alternating current to alternating voltage converter was presented. The mathematical model was derived and it was shown that the transformation from alternating current to alternating voltage could be done. A digital PID controller implemented with the aid of a PIC18F452 microcontroller was introduced. A flowchart of the program as well as the listing of the c-program has been included.

In the next chapter the simulation models done on both the TRAFTAP systems are shown. The results obtained from some of the simulations that were done are shown and conclusions drawn.

A possible alternative for the two zener diodes is a MOSFET used as a single zener diode. This can be done because modern MOSFET's are avalanche tested at their forward break over voltage and behave like zener diodes in this region. The zener diode is shown in the symbol of these avalanche tested MOSFET's. Although theoretically a 500V thyristor could do the job on its own without the trigger circuit, in practice it is hard to find thyristors with such low forward break over voltages. because technology has moved on and thyristors with high break over voltages such as 800V, 1200V and 1600V are now available. This has forced the use of a trigger circuit to ensure a lower threshold voltage on the AC crowbar that is lower than the forward break over voltage of modern thyristors.

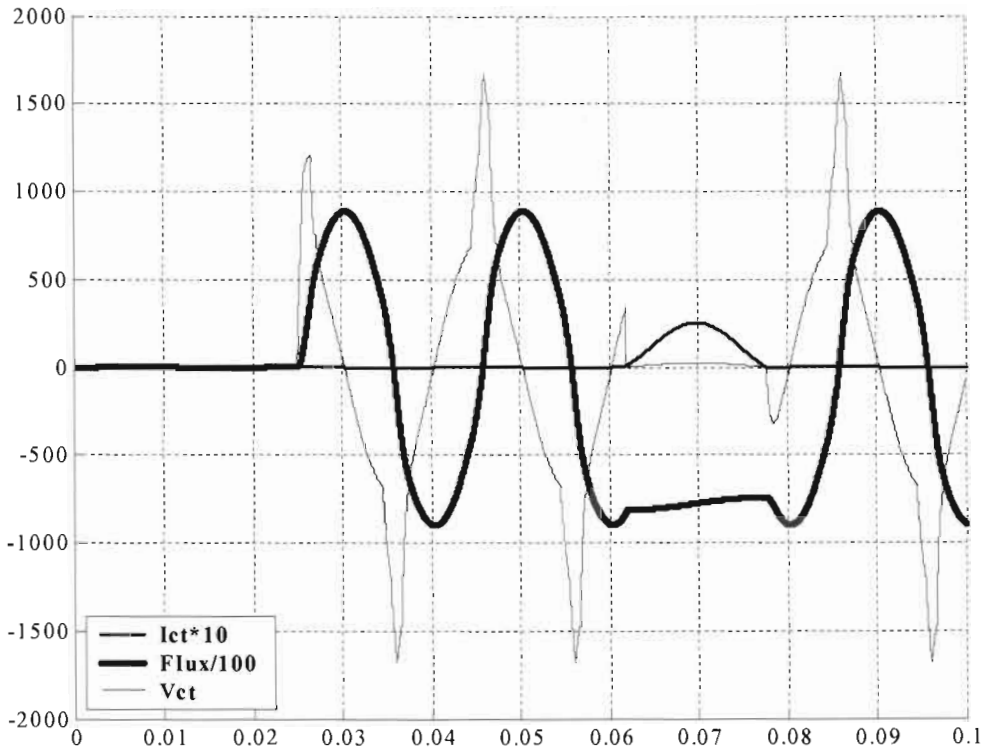


Figure 39: AC crowbar action on CT secondary current, pu flux and output voltage

A practical circuit and simulation on MATLAB have shown that only one thyristor will be triggered in every cycle since the saturation experienced by the CT core under these circumstances is such that the $d\varphi/dt$ is not enough to produce secondary

voltages high enough to reach the predetermined values since the CT core is operated close to the flux saturation values.

The results in Figure 39 show that only one thyristor will be triggered per cycle, since the CT core flux is operated very close to its saturation level during the time that the thyristor is ON. When the thyristor switches OFF, the CT is pushed back into saturation and the $d\varphi/dt$ is therefore limited. This results in an induced voltage on the CT secondary that is not high enough to trigger the second thyristor in the AC crowbar. It is argued that although only one thyristor switches ON per cycle, both thyristors should be included in the AC crowbar so that any voltage high enough to trigger the AC crowbar should activate it no matter what its polarity.

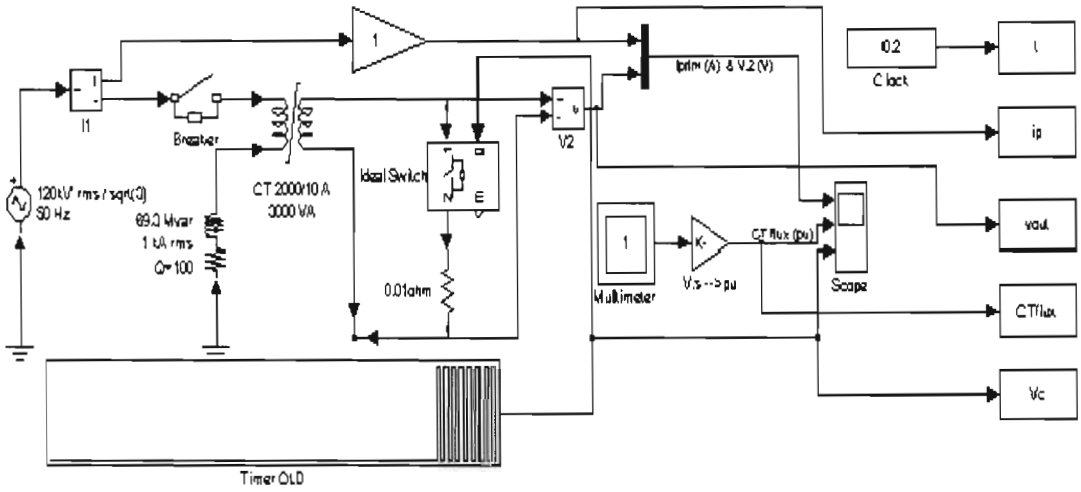


Figure 40: Simulation model used to investigate CT saturation

4.2 CT saturation

A question that is regularly asked during discussions about the TRAFTAP is what the influence would be of transients on the power line that cause saturation of the CT. This saturation could be the result of lightning strikes on the line or of sections being switched in or out. A modification of the model (Figure 40) was used to investigate this question.

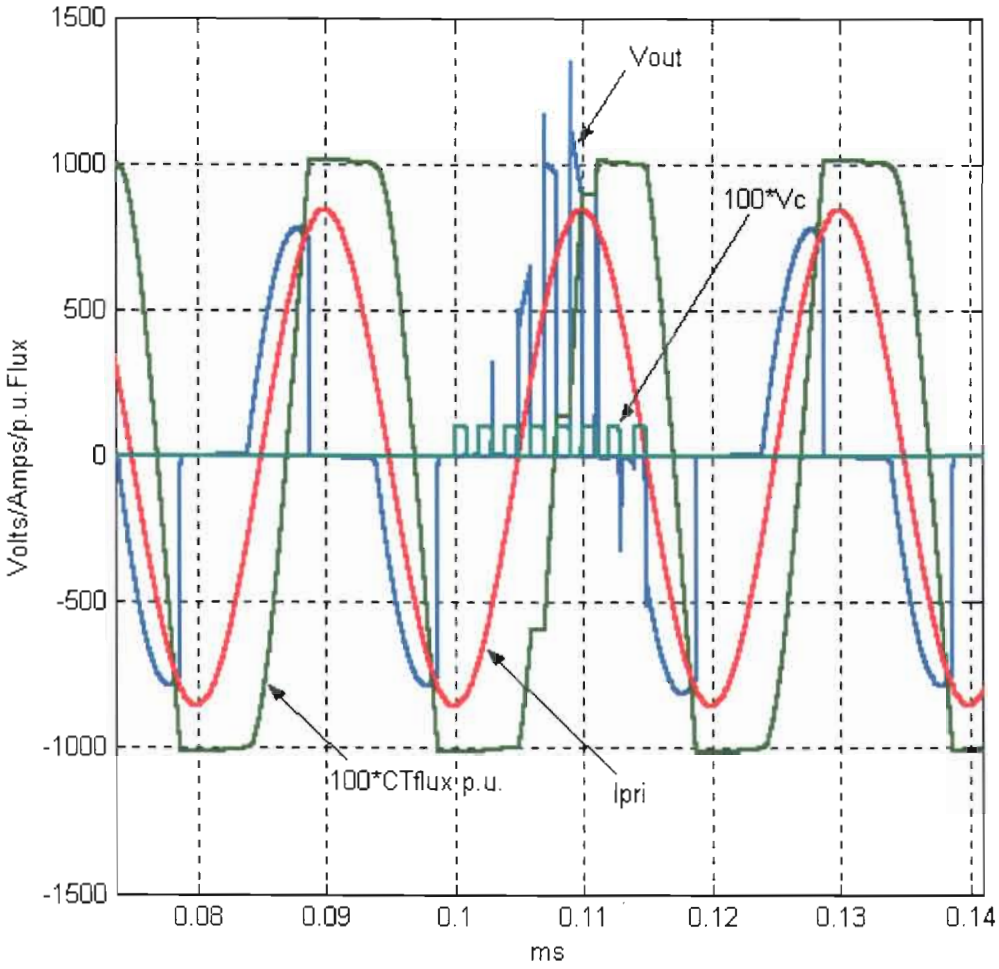


Figure 41: CT output under transient conditions causing saturation

Figure 41 shows the primary current, the flux density, the switch control voltage and the output voltage under transient conditions. The CT flux density is modelled as saturation at 10 times the normal flux density. As can be seen from the graphs in Figure 41 the control voltage only switches from time t = 0,1 up to 0,116 ms in order to evaluate the CT output during conditions of saturation and of non-saturation.

In order to show all waveforms on one axis, the relative sizes of the flux density and control voltages have been multiplied with a factor of 100 so that they are visible. When the first three pulses of the control switches the main switch, no effect is seen in the output waveform since at this stage the CT is in negative saturation. However,

switching the main switch ON and OFF during the time that the CT flux density is changing from negative to positive saturation, generates an output voltage during the times that the switch is ON. The moment the CT goes into positive saturation no output voltage is produced by the same action. This means in effect that the storage capacitor in such a system would have to be large enough to sustain power to the load through a transient condition otherwise power to the load will be interrupted as soon as the storage capacitor voltage becomes too low.

4.3 Step response of the TRAFTAP1 system

The step response of the system was evaluated with the simulation program SIMetrix41. Although the UC3842 is available in SIMetrix41, the control voltage is internally derived and kept constant at 2,5 V. This makes it impossible to evaluate the system with a step change in the input variable. The action of the IC was replaced with a dependant current source and the chopper was modelled with a dependant current source, which simulated the average output of the CT, bridge rectifier and switch S_1. The simulation model is shown in Figure 42. The current in the simulation model was limited to 10 A.

As can be seen in Figure 43, the response of the system to a step change causes negligible overshoot and settling time. It takes 5,5 ms for the load voltage (over storage capacitor) to reach its controlled value after application of a unity step input. A step in the load current from 0 to 7 A at time t = 6 ms up to 6,5 ms also causes an adequate response from the controller and no instability is observed. The current supplied from the CT was limited to 10 A.

4.4 Simulation with the UC3842 as the controller

Simulation of the circuit with the UC3842 was done on SIMetrix41 simulation software. The simulation model is shown in Figure 44.

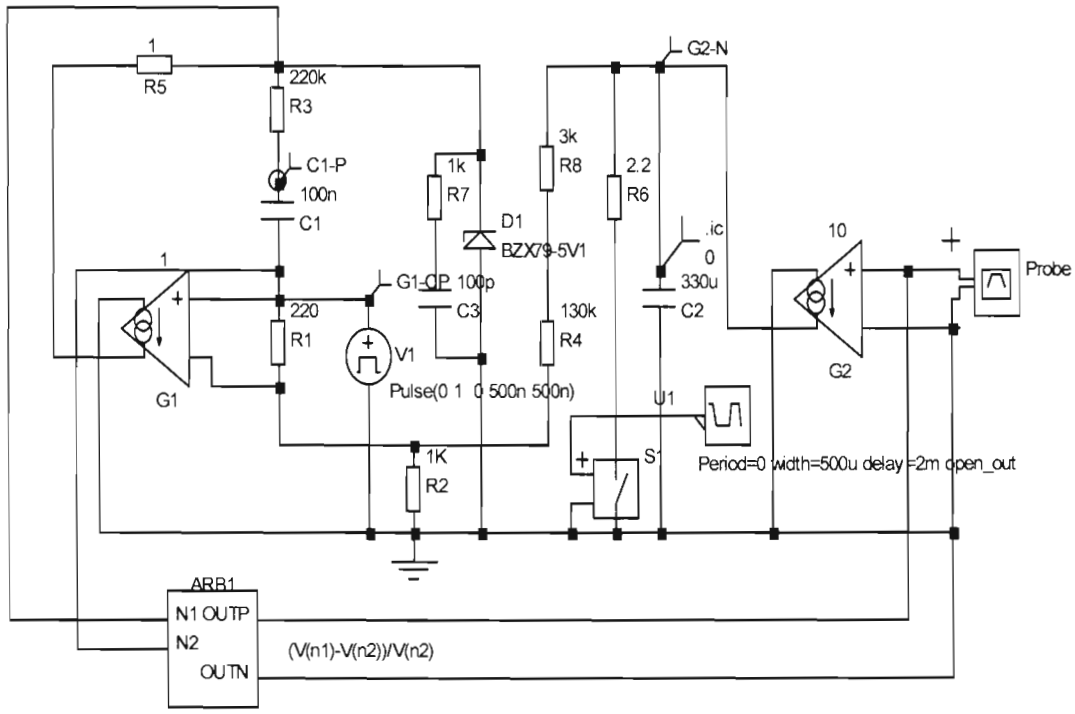


Figure 42: Simulation model of the TRAFTAP1 system

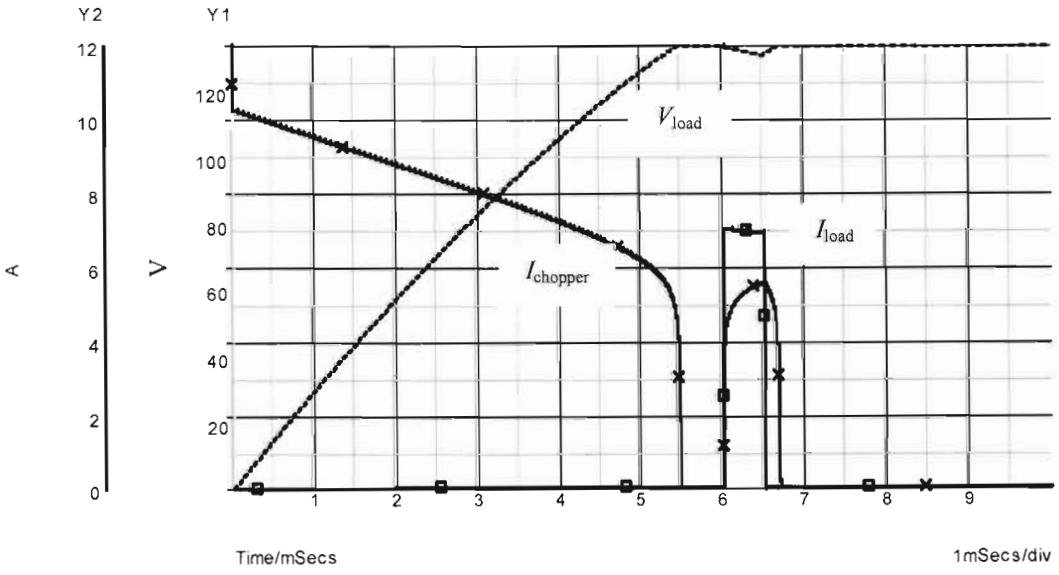


Figure 43: Simulation results of system for step input and load step

The AC supply line was modelled with a voltage controlled current source fed by a sine wave of unit amplitude. The current source has a gain of 1000, which gives a primary current of 707 A rms flowing in the primary of the CT. The CT has a turns ratio of 1:100 which results in a secondary rms current of 7,07 A.

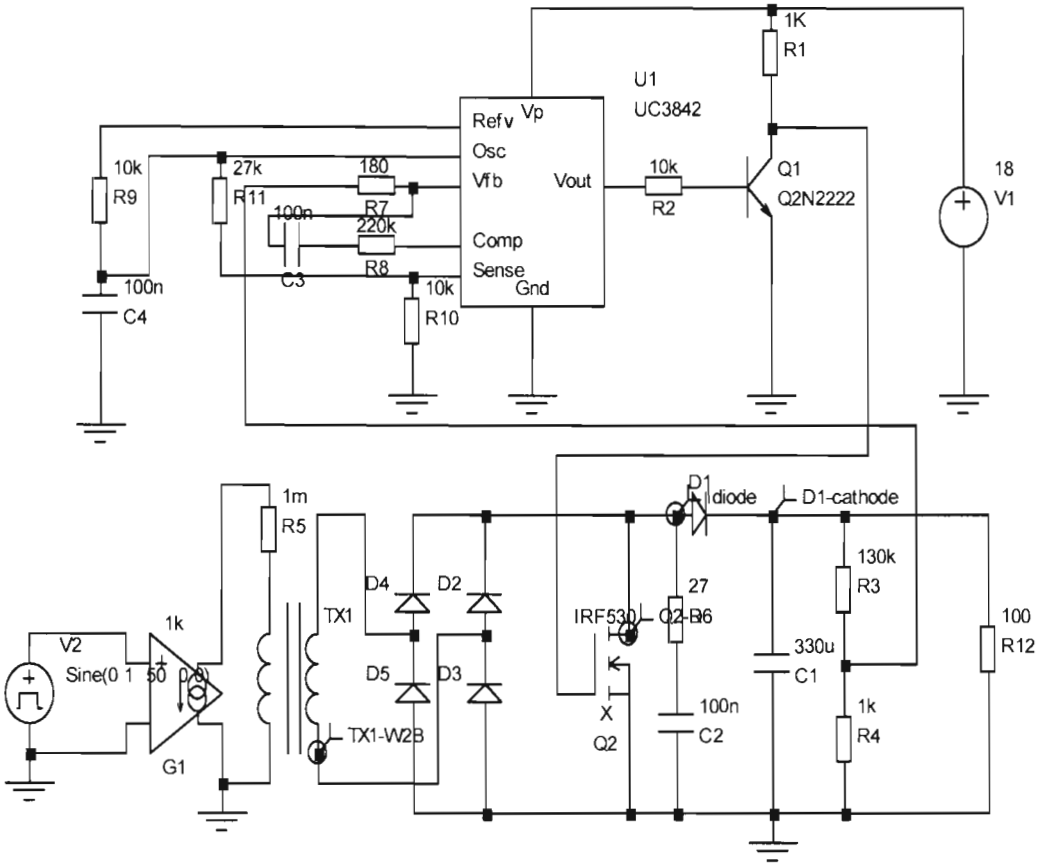


Figure 44: Simulation model of TRAFTAP1 using UC3842

The controller action can clearly be seen in Figure 45 where the duty cycle of the current through the diode is varied to compensate for the pulsating nature of the supply current. The average load current was kept constant at about 3 A while the input current being a half-sinusoid varied from zero up to 10 A peak. As can be seen the load voltage was kept fairly level by the controller. No instability occurred.

The primary voltage over the CT has raised many a question at conferences where

this work was presented. Simulations done reveal that the primary voltage is small in comparison with the voltages that do exist in a transmission line system. Figure 46 shows the voltage reflected into the primary circuit to be about 3 V rms. The voltage is directly related to the power that has to be supplied by the CT. The CT power input is equal to the power losses in the CT, plus the power delivered to the load.

$$P_{in} = P_{loss} + P_{out} \tag{175}$$

where

P_{in} is the power supplied to the CT,

P_{loss} is the power taken by magnetization and resistive losses in the CT and

P_{out} is the power delivered to the CT load.

The power input to the CT is a function of the primary current and the primary voltage. Thus

$$P_{in} = V_{pri} \times I_{pri} \tag{176}$$

In order to deliver power from the CT, the volt-amp product at the input to the CT must be balanced with the volt-amp output plus any losses in the CT. Since the current here is not determined by the load, but is a given, it means that the primary voltage will vary as the duty cycle of the switch is varied.

Analysis of the CT primary voltage and primary current reveals that there is a sinusoidal pedestal on which the chopped portion of the primary voltage is superimposed (Figure 47). The pedestal is 90 degrees out of phase with the primary current indicating that it represents that portion of the primary voltage drop, which is related to magnetization.

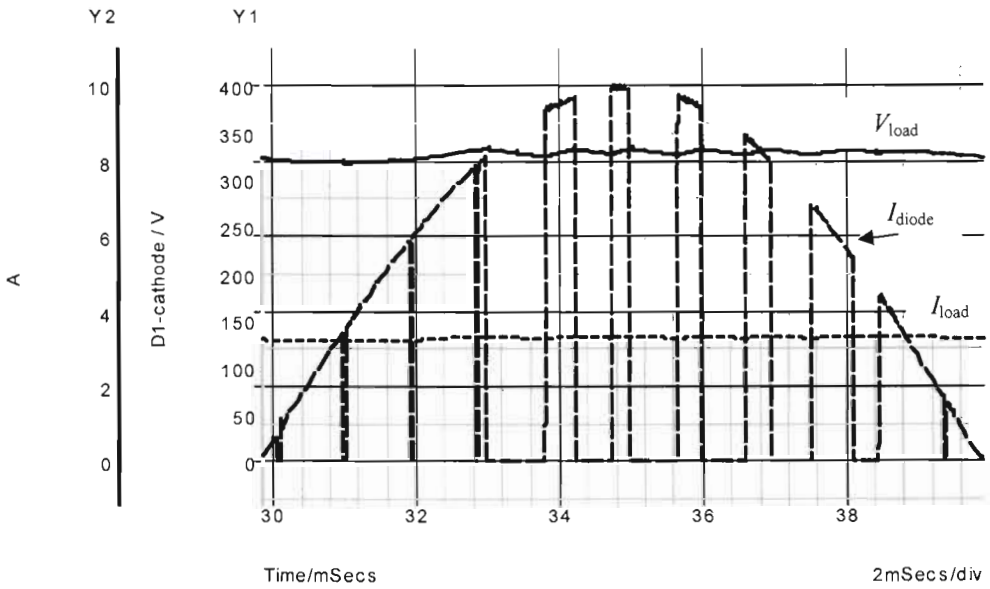


Figure 45: Controller action illustrated

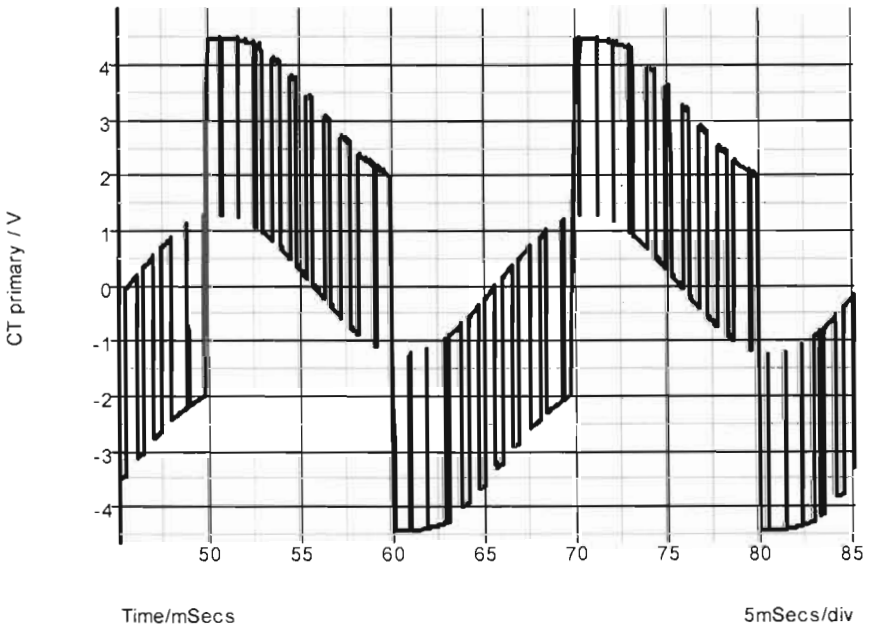


Figure 46: CT primary voltage

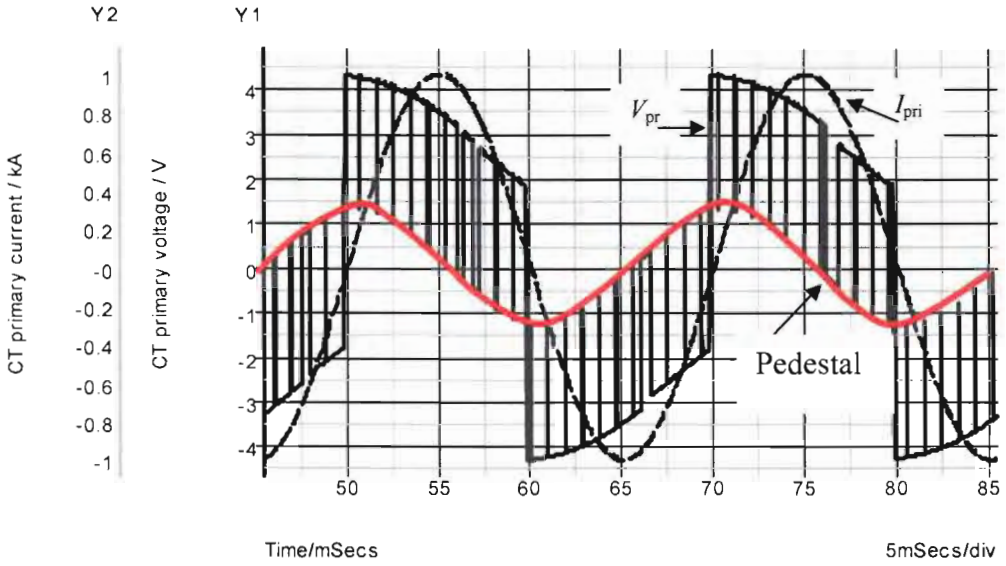


Figure 47: CT primary current and voltage

4.5 Simulations of the TRAFTAP2 system

The Proteus software package allows for a microcontroller program to be evaluated in a circuit containing a model of the microcontroller. Using this package, the TRAFTAP2 system was modelled and various simulations done to evaluate the controller action. Figure 48 shows the PIC microcontroller and the TRAFTAP2 system model ready for simulation.

Forcing the duty cycle to be about 35%, initially restricts the output voltage to a safe value for the first three cycles after switch-on (Figure 49). Subsequently, the integral action brings the output voltage up to the regulated value without any overshoot or ringing.

The CT secondary is fed to a filter which prevents the higher frequencies contained in the CT secondary waveform to reach the load.

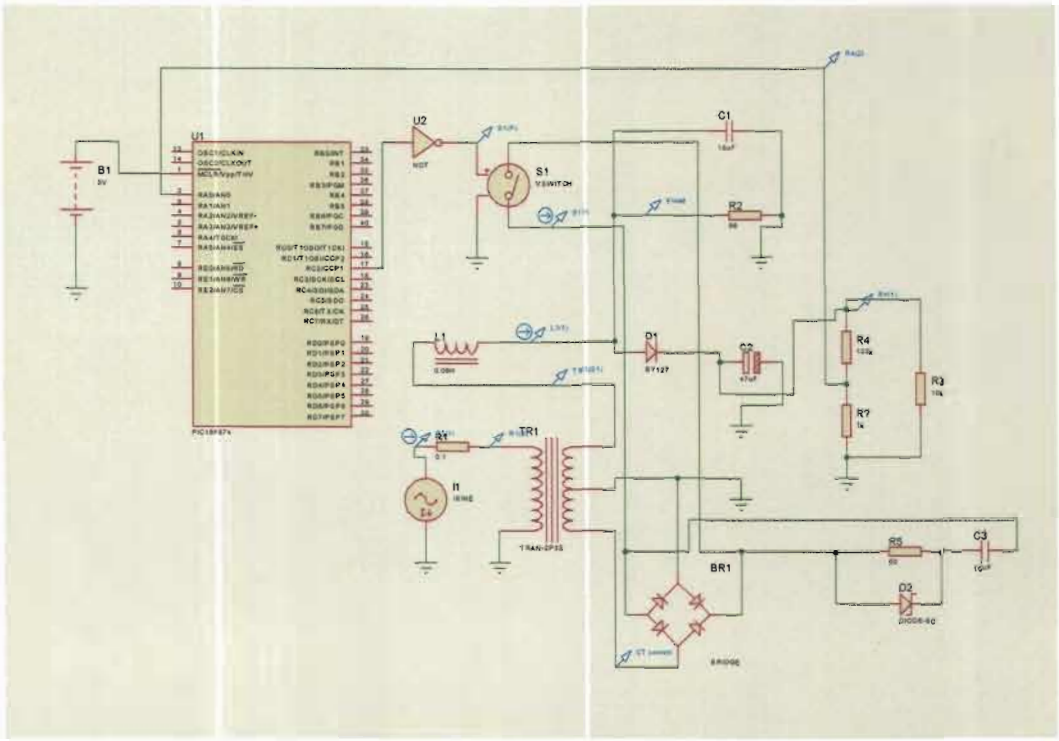


Figure 48: TRAFTAP2 simulation model on Proteus software

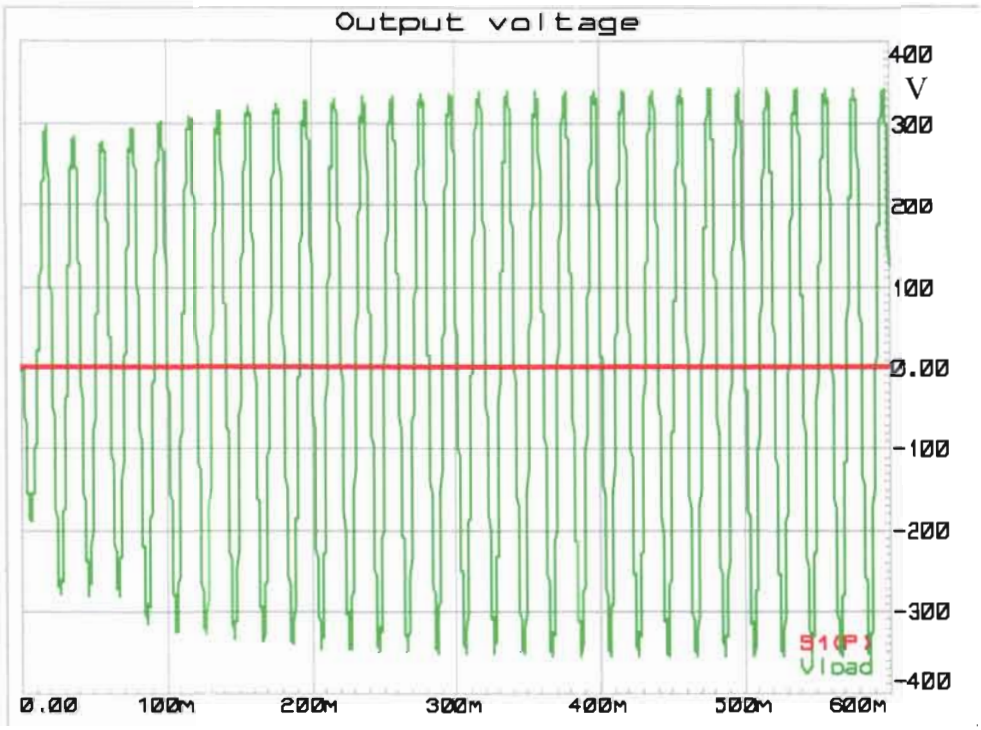


Figure 49: Load voltage at start-up

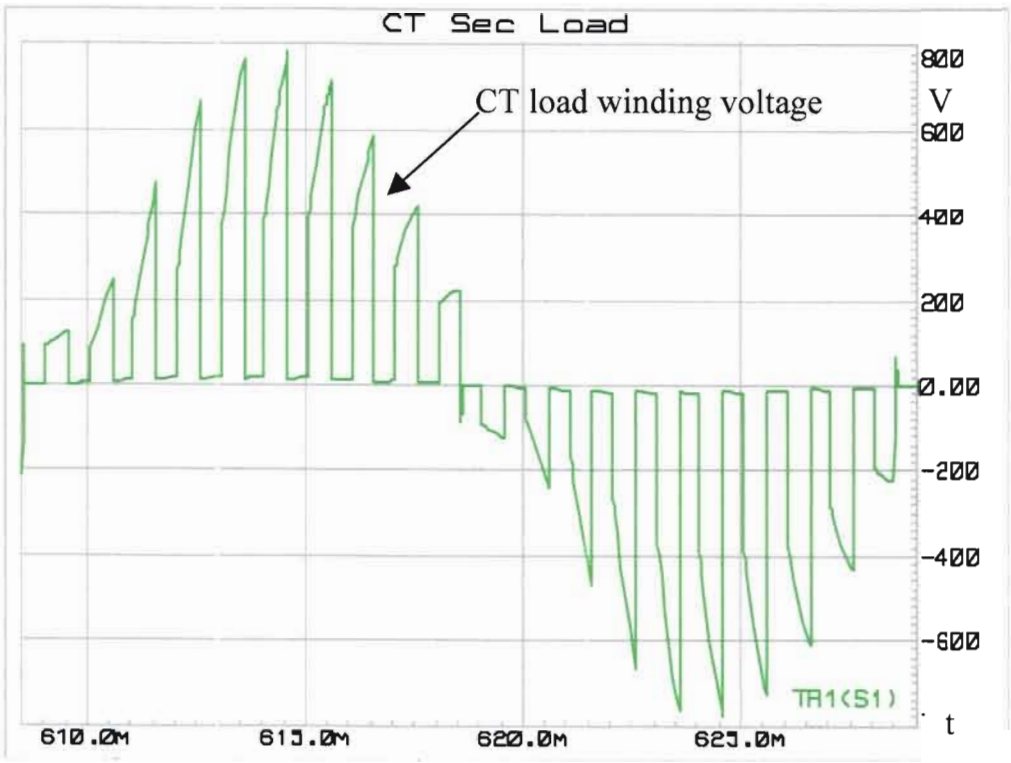


Figure 50: CT secondary output voltage

Figure 50 shows one cycle of this chopped waveform. Comparison of this waveform with that in Figure 35 shows that it is indeed the output waveform of an ETRC system. The removal of the higher frequencies by the filter leaves only the fundamental frequency, which in this case is 50 Hz. The voltage waveform after the filter, i.e. over the load, is shown in Figure 51. All the high frequency components have been removed. The small ripple superimposed on the sinusoidal waveform is due to the low switching frequency, which was used to be able to better illustrate the process. Increasing the switching frequency would reduce this ripple to be negligible. Also shown is the PIC PWM output on which the duty cycle can be observed. The spectrum of the output voltage is shown in Figure 52. The modulation products of the switching frequency and the utility frequency are visible at 950 Hz as well as at 1050 Hz. However, compared to the amplitude of the fundamental these products are negligible.

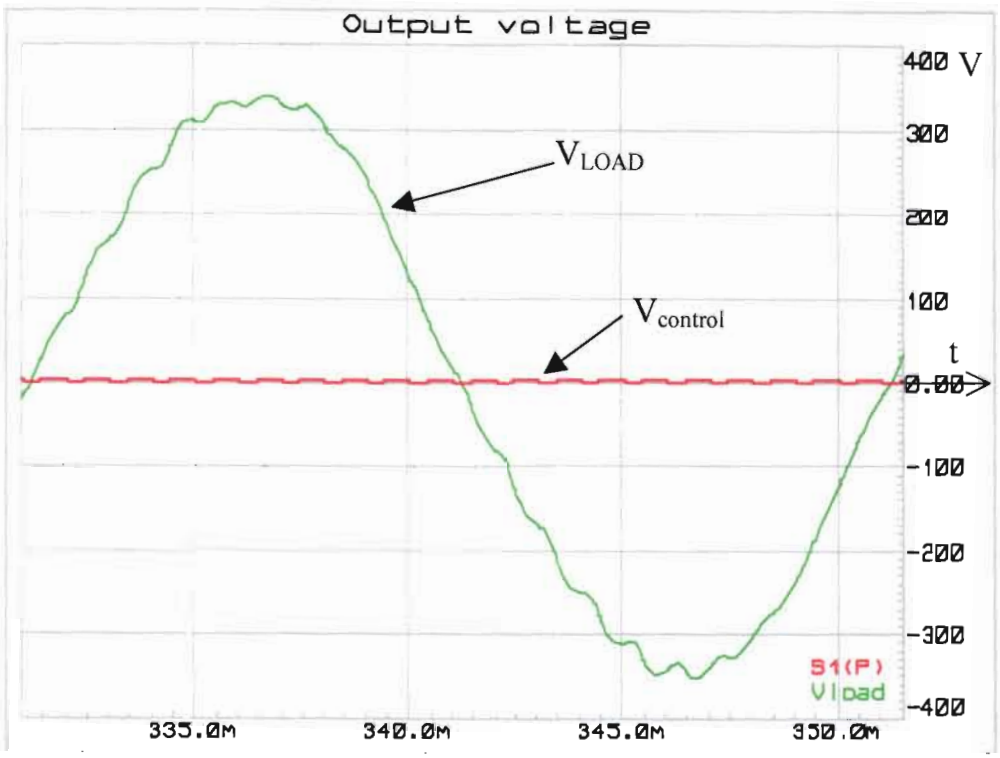


Figure 51: TRAFTAP2 output voltage waveform

The action of the controller at start-up can be further explained by examining the feedback voltage (Figure 53). For the first three cycles the output voltage is restricted. However, this does not prevent an initial voltage spike during the first cycle, but the spike is still within acceptable limits. After the first three cycles, the PID controller action is allowed to go its course and brings the output voltage to its regulated value of about 235 V (rms). When the regulated output voltage is reached, the feedback voltage sampled by the PIC microcontroller is about 2,5 V, which is the same as the software set point. When the main switch is ON, the control winding current is equal to the primary current times the turns ratio of the CT. During this time, the filter inductor supplies the current flowing in the load winding. When the main switch is OFF, no current flows in the control winding and the current in the load winding is increased. The filter inductor however prevents a rapid increase. During this OFF time energy is transferred to the filter inductor to be released during the time that the main switch is switched ON again.

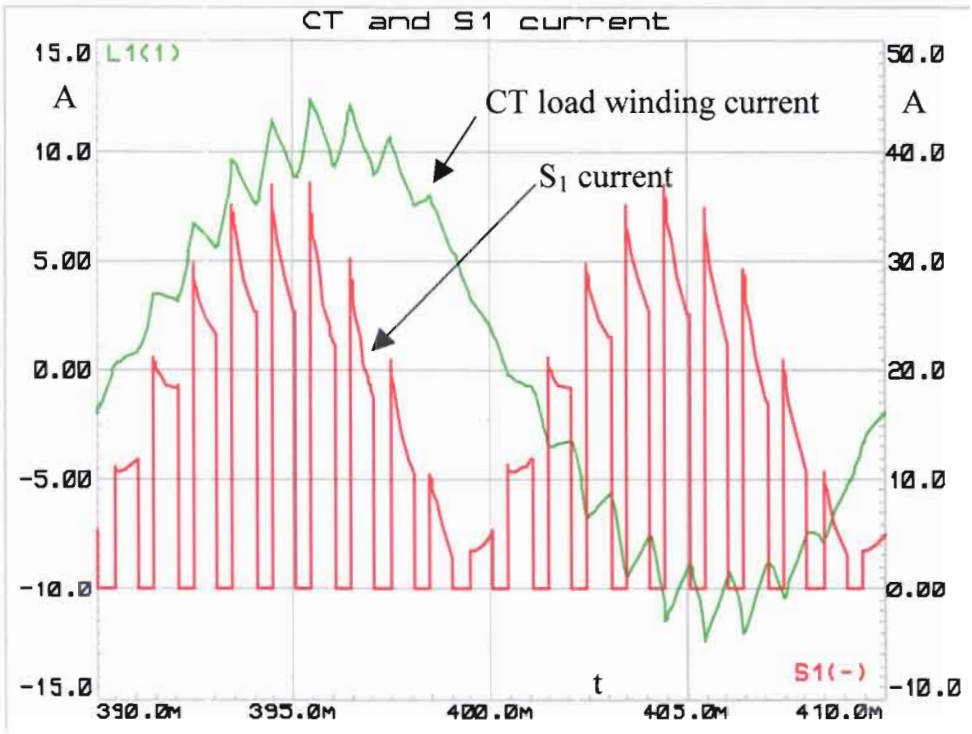


Figure 54: Main switch current and CT load winding current

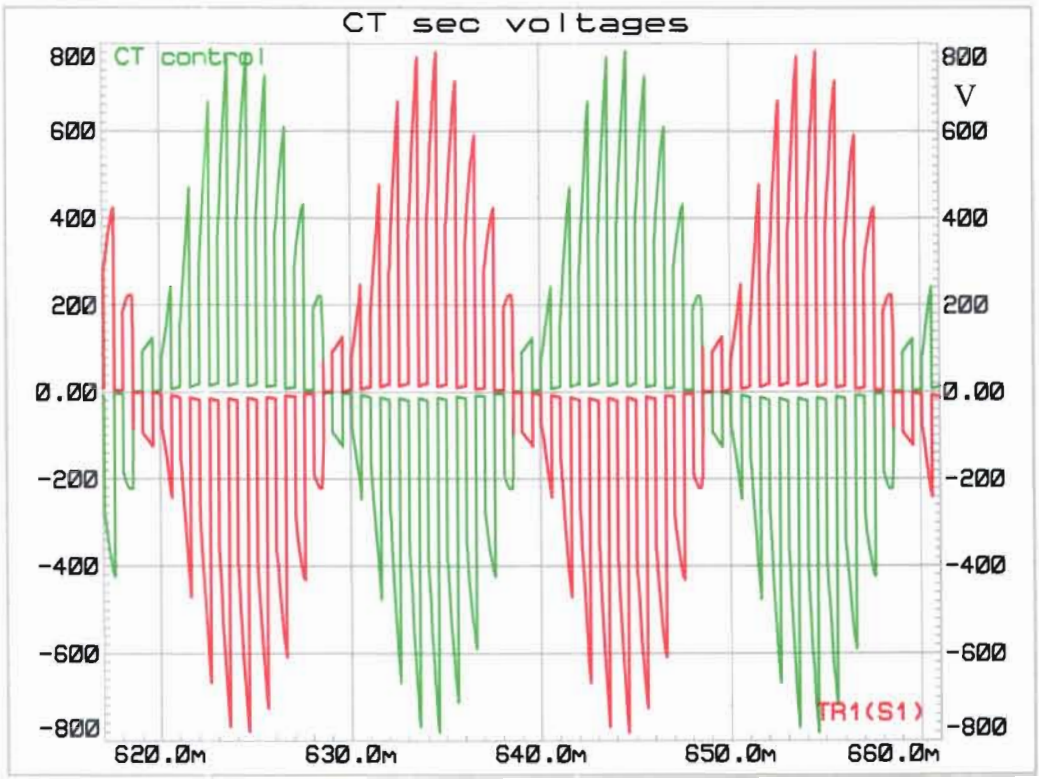


Figure 55: CT voltages of control and load windings

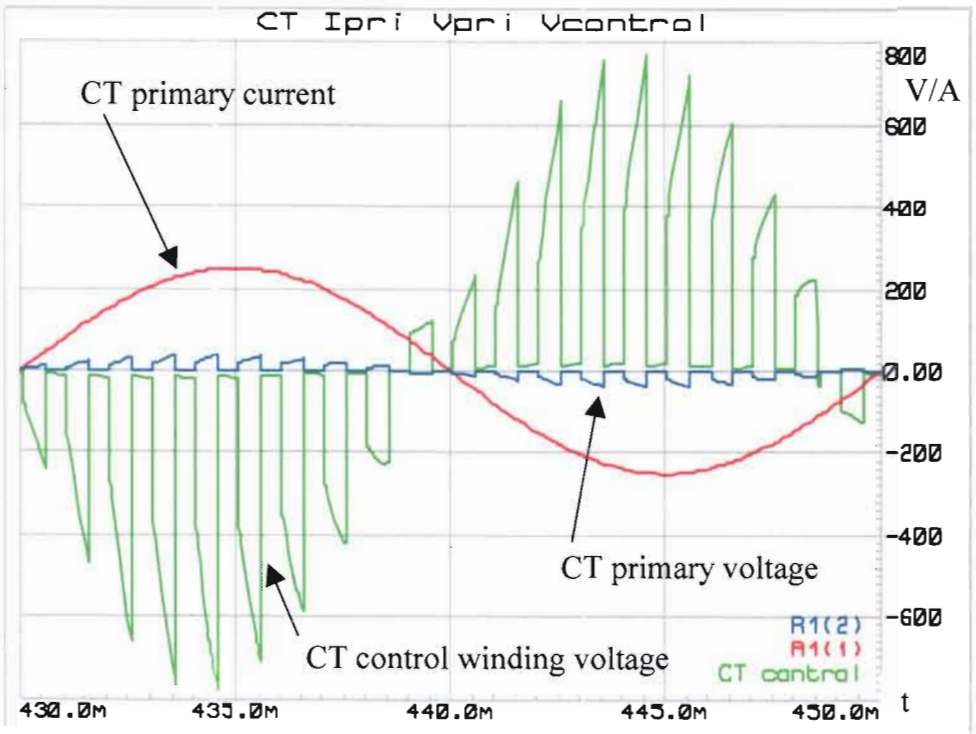


Figure 56: CT primary voltage, current and control winding voltage

Applying a short (main switch is ON) to the control winding also causes the voltage on the load winding to reduce to a minimum. This can be seen on the two graphs shown in Figure 55, which are mirror images of each other since the transformer model used for the CT in PROTEUS software does not have a transformer model with two separate secondary windings. The purpose of the simulation is however to show that the two voltages follow each other in magnitude.

In Figure 56, the red trace is that which is the voltage measured over the CT primary, the blue trace is the control winding voltage and the green trace is the CT primary current. From this graph it can be seen that switching the main switch ON, causes the control winding voltage and the primary voltage to reduce to zero. This corresponds to what happens to the load winding voltage as shown in Figure 55.

4.6 Summary

The results of many simulations to illustrate the various aspects of the TRAFTAP systems were presented. These included stability issues. It has also been shown that the simulation results agree favourable with the mathematical models presented in the previous two chapters. In the next chapter, the practical models and the results obtained with these models are presented.

Chapter 5 Experimental models and results

The results obtained from two experimental models that were built are presented. The first model was that of TRAFTAP1 and the second was TRAFTAP2. The controller of TRAFTAP1 was analogue and that of TRAFTAP2 digital.

5.1 Measurements made on TRAFTAP1 experimental model

A CT experiences a high rate of flux change when the secondary is open circuit without an AC crowbar to protect it. This leads to high voltage peaks as shown in Figure 57. The CT used for the experimental set-up of TRAFTAP1 was subjected to a primary current of 4 A peak without the AC crowbar and produced voltages of up to 780 V peak indicating the need for a protective crowbar circuit (Figure 6)

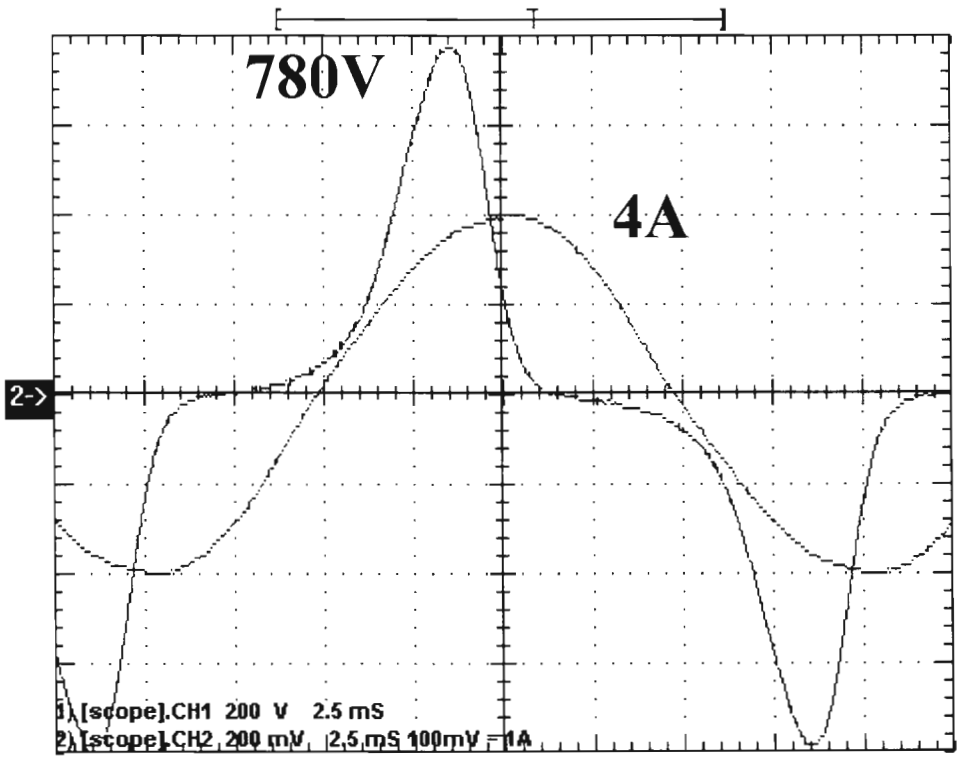


Figure 57: CT secondary voltage when open circuit

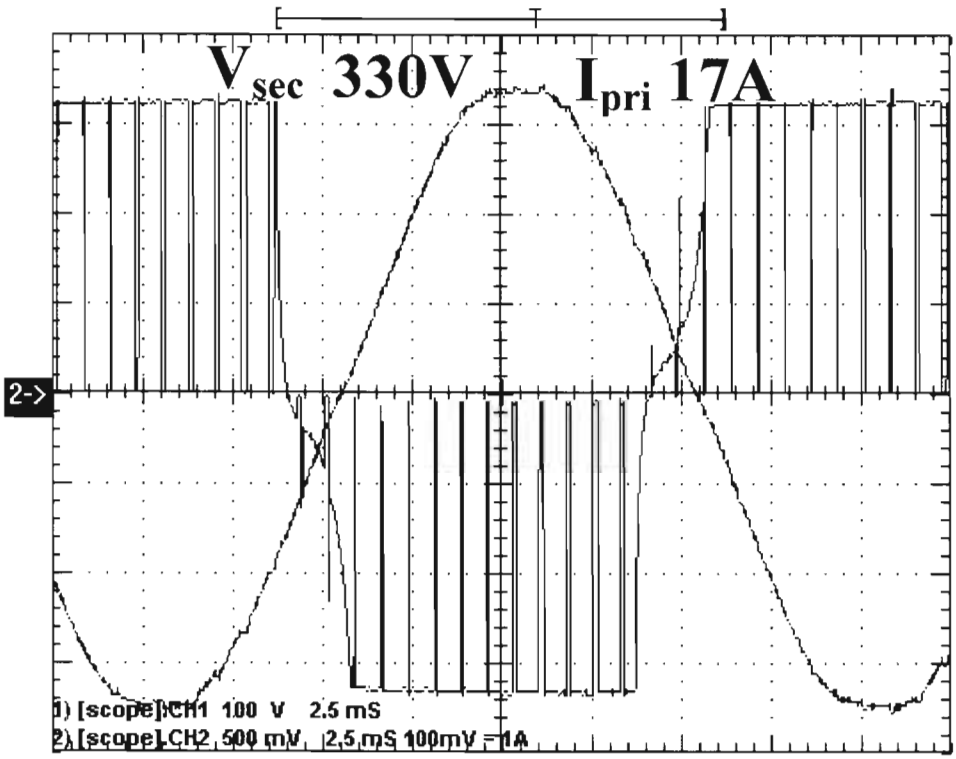


Figure 58: CT secondary loaded

The action of the PWM PI controller on the CT secondary voltage is shown in Figure 58. The secondary voltage rises to the DC link voltage and is clipped at the regulated value. In this experiment, the regulated value was 330 V. The duty cycle of the main switch in TRAFTAP1 is at a minimum just after the primary current goes through zero, since the DC link capacitor looses some of its charge when the primary current is less than the nominal current of the load. As soon as the DC link voltage has reached its regulated value, the duty cycle of the main switch is increased to a value, which just maintains equilibrium between the diode current and the load current. In the scope measurement shown in Figure 58 the CT primary current was 17 A peak.

The influence of TRAFTAP1 on the primary current is illustrated by the oscilloscope measurement shown in Figure 59.

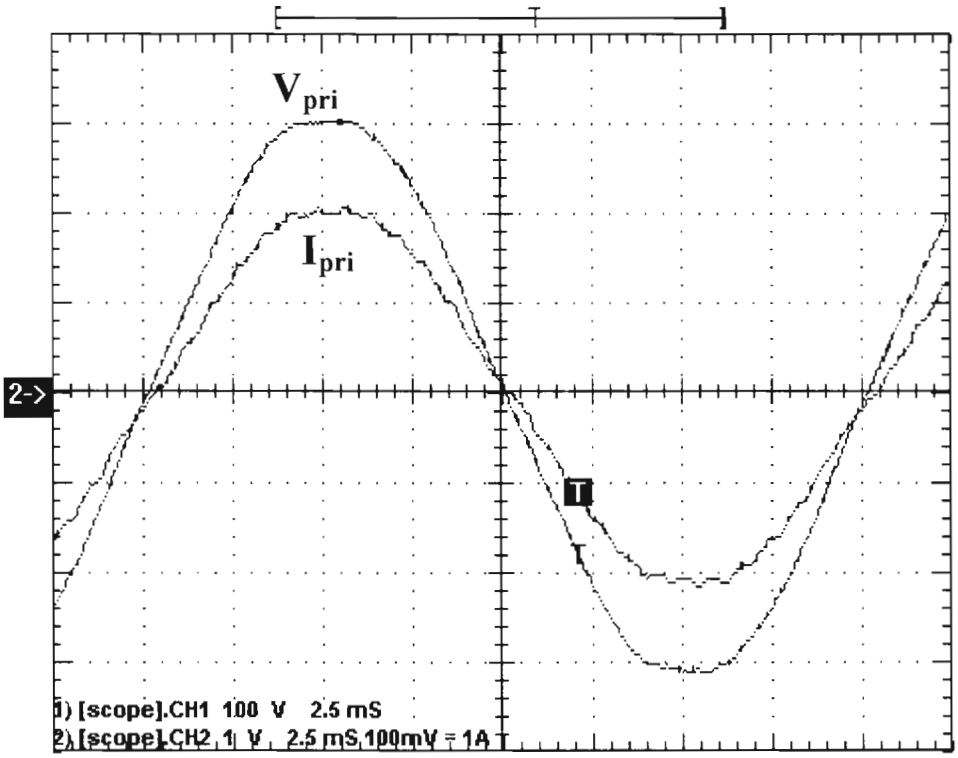


Figure 59: Current and voltage of the primary circuit

The primary current has a ripple superimposed on the sinusoid caused by the voltage reflected into the primary circuit via the CT which in the experimental set-up, is a reasonable percentage of the applied primary voltage. In this case a 300 V peak sinusoid is applied to produce a 10 A peak current in the primary circuit. The CT primary voltage is about 15 V peak (Figure 60), which is about 5 percent of the applied primary circuit voltage. When comparing this CT primary voltage to that on a transmission line (400 kV), the CT primary voltage becomes, percentage-wise, virtually zero and the influence on the primary line current will be unnoticeable. This means that it is possible to install many TRAFTAP1 systems on a line without causing a noticeable influence. Furthermore, the influence will be reduced by the fact that the individual TRAFTAP1 systems will not be synchronized with each other and will therefore tend to present an averaged parasitic load.

The CT primary voltage is that reflected from the CT secondary (Figure 60).

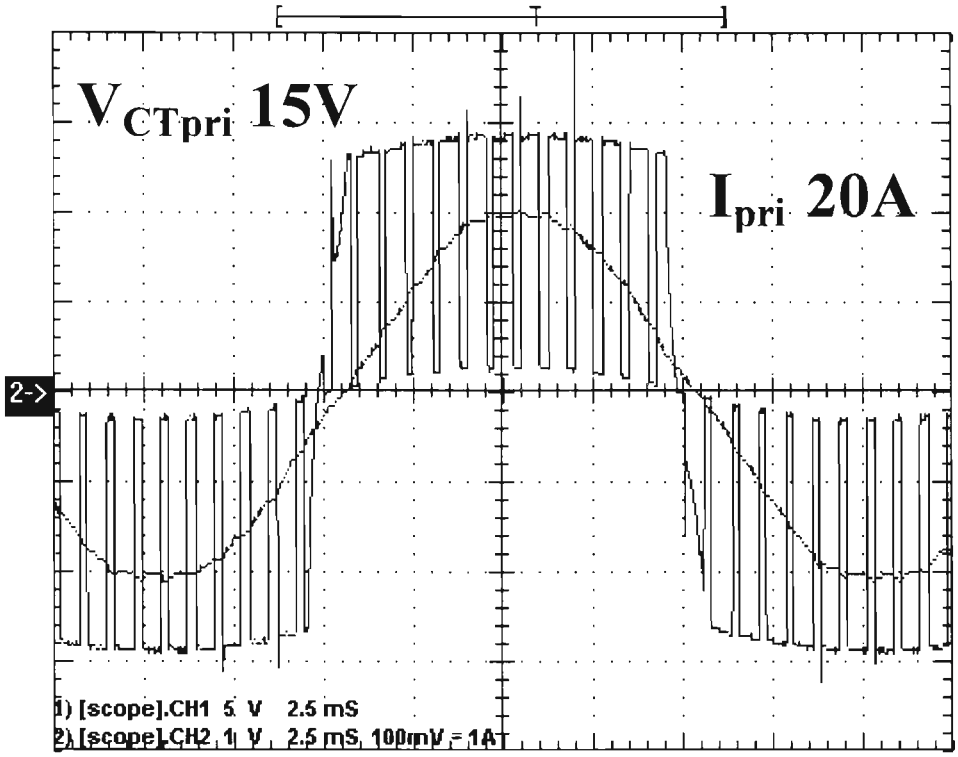


Figure 60: CT primary voltage and current waveforms

Two conditions can exist: the main switch is ON and the main switch is OFF. While the switch is ON, the voltage on the secondary is the combination of two forward biased diode volt-drops, the main switch on-state volt-drop and the volt-drop caused by the resistance of the secondary winding. This voltage divided by the turns-ratio of the CT is reflected into the primary circuit. Added to this is the volt drop over the resistance of the primary winding and the magnetizing inductance. This can be seen by the sinusoid formed by the lower points of the CT primary voltage (Figure 60). While the switch is OFF, the voltage reflected into the primary circuit is the sum of three diode forward volt drops, winding resistance volt drop and the DC link voltage divided by the turns ratio of the CT. Added to this is the primary side volt-drop due to magnetizing inductance and resistance. The peak of this voltage is just below 15 V. The primary current ripple is also noticeable on the waveform shown in Figure 60.

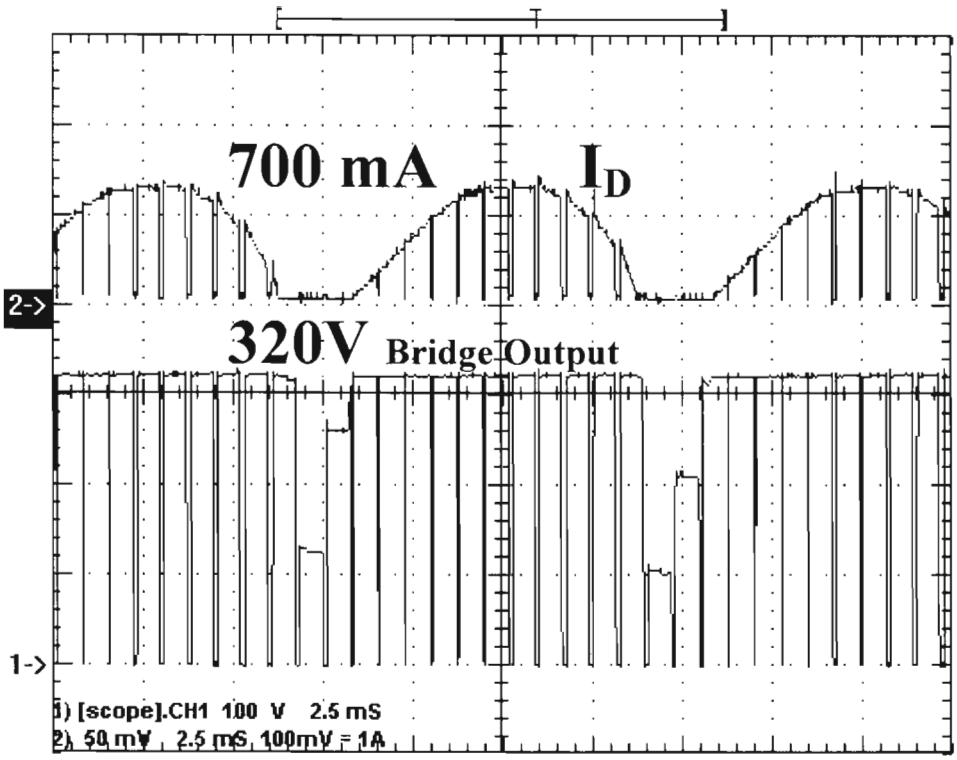


Figure 61: Diode current flowing towards DC link capacitor

The main diode current in the TRAFTAP1 circuit only flows when the energy in the CT is able to produce a secondary voltage in excess of the DC link capacitor voltage. The secondary current of the CT flowing through the diode follows the envelope of a half sinusoid produced by the rectifying action of the diode rectifier. Near the natural current zero's, the energy in the CT is insufficient to forward bias the main diode as can be seen by the voltage pulses which do not reach 320 V (Figure 61). No secondary current flows during these periods when the main switch is OFF. The influence of this on the primary side of the CT cannot be distinguished (see Figure 59 and Figure 60) and can therefore be ignored. A circuit detecting this situation can however be incorporated to switch on the main switch for the remainder of the switching period if the CT secondary voltage does not reach the DC link voltage immediately after the main switch is switched OFF.

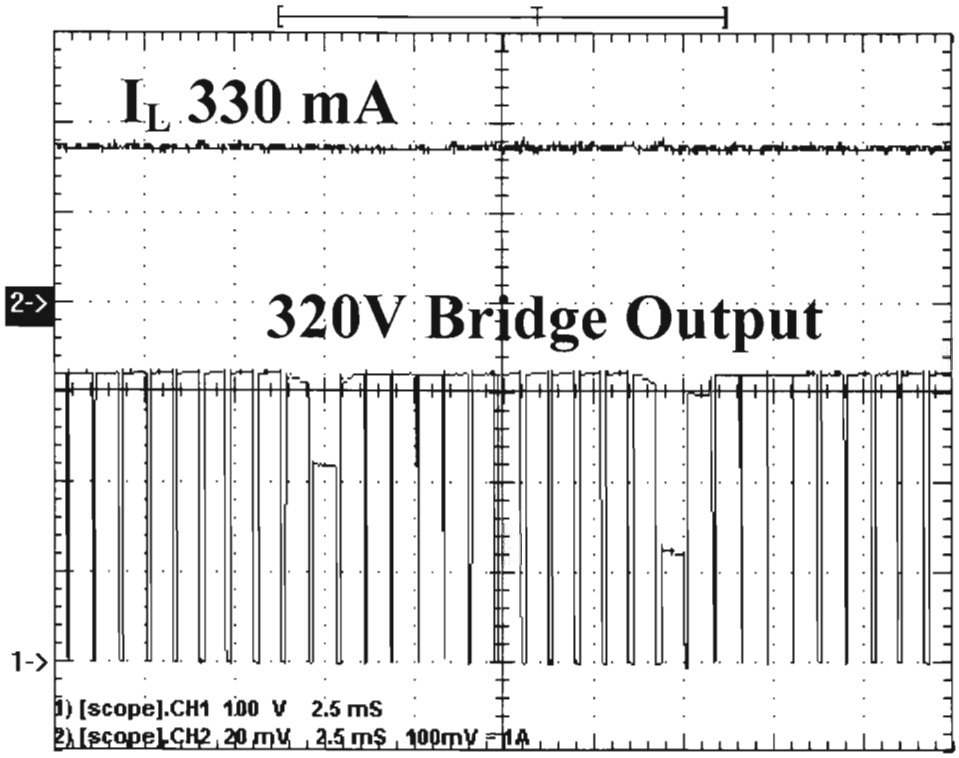


Figure 62: DC link load current and the bridge voltage

The DC link load current remains constant even during the time that the CT secondary voltage fails to forward bias the main diode. This means that the DC link presents a regulated voltage to the load. The power transferred to the load in this case was

$$P_{Load} = V_{DC} \times I_{Load} \tag{177}$$

$$P_{Load} = 320 \times 330 \times 10^{-3} = 105,6 \text{ W} \tag{178}$$

This proves practically that it is possible to transfer power from a CT to a load.

5.2 Measurements made on TRAFTAP2 experimental model

A switching frequency of about 1 kHz was chosen so that the action of the system can be shown more clearly. In Figure 63, the top waveform is the voltage over a resistive load and the bottom one is that which is applied to the gate of the main switch. The main switch is ON when the voltage applied to its gate is HIGH and OFF when the voltage is LOW. During the ON time, current is diverted away from the CT secondary feeding the load. On the graph it can be seen that the instantaneous amplitude of the load voltage is reduced during the times that the switch is ON. When the switch is OFF, the instantaneous voltage over the load increases. From a load point of view, the wave shape can be made to approximate a sine wave more closely, by using a higher switching frequency. The CT primary current in Figure 63 was 4,5 A.

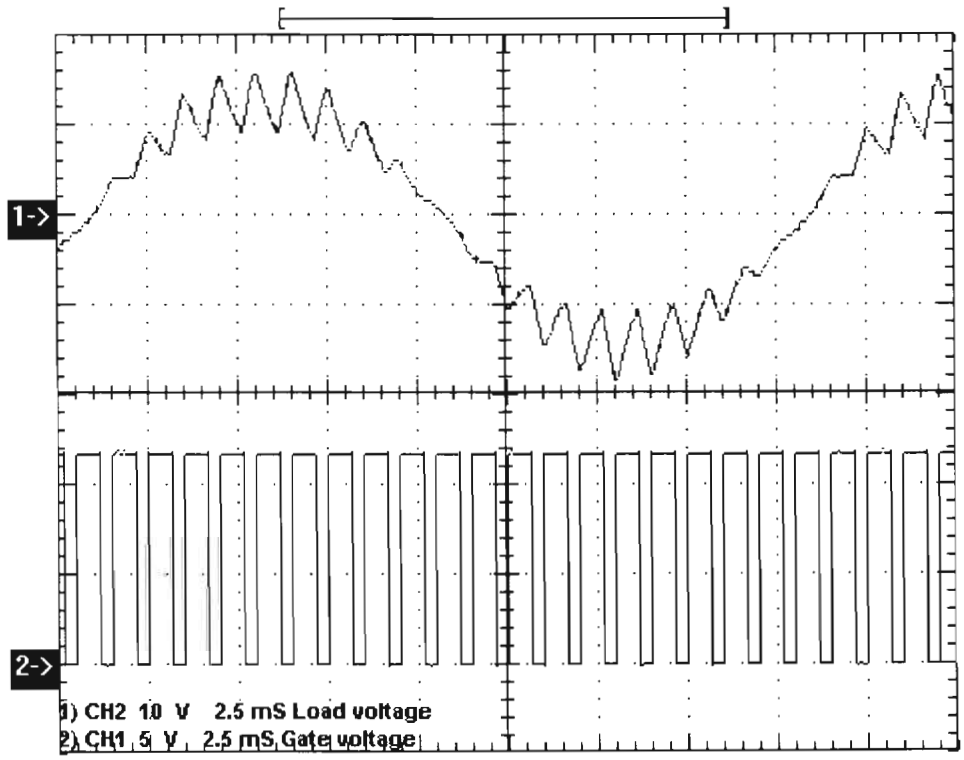


Figure 63: TRAFTAP2 main switch gate voltage and the load voltage

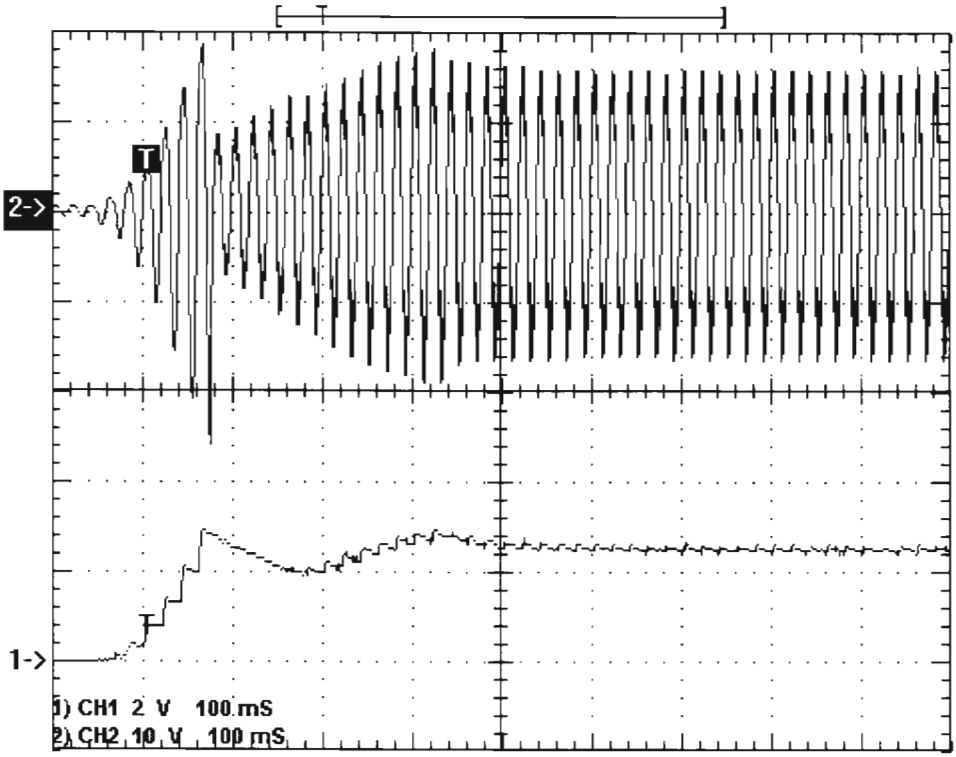


Figure 64: Action of the PID controller

The action of the PID controller is to keep the output voltage constant under varying input current and load conditions. Figure 64 shows the load voltage and feedback voltage at start-up. The primary current was increased from zero up to 4,5 A. Chopping action only starts when the sampled voltage exceeds 2,5 V (which is the set point voltage). The controller was programmed to prevent a voltage surge. Therefore, it immediately increases the duty cycle and loads the integral register with a negative value. The decline in amplitude and the gradual rise in amplitude until it settles at the value corresponding to a set point of 2,5 V is shown with the trace of channel 2 in Figure 64. Channel 1 in the same figure is the feedback voltage, which is sampled by the PIC microcontroller. The feedback voltage is derived from the load voltage via a half wave rectifier and a smoothing capacitor. It acts as a load voltage peak detector. During the time immediately after an over voltage detection, the load voltage peaks are less than the smoothing capacitor voltage and the voltage then declines according to the time constant formed by the capacitor and voltage

divider circuit.

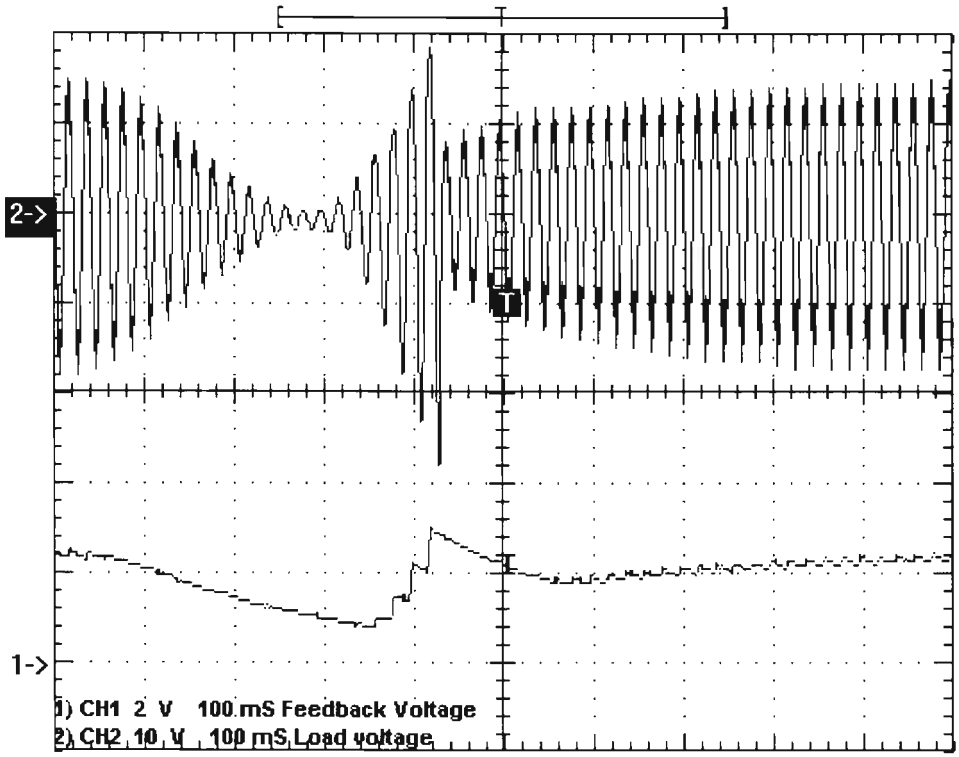


Figure 65: PID action during a dip in the primary current

The PID controller prevents a surge in the load voltage to dangerous levels when the load voltage exceeds the set point voltage. A dip in the primary current causes the controller to reduce the duty cycle of the main switch to zero in an attempt to sustain the power to the load. A surge in primary current after the dip, causes the load voltage to quickly increase beyond the set point value, since controller action is only activated according to the peak of the previous cycle. This is according to the control philosophy of ETRC, which is to adjust the duty cycle of the current cycle according to the error value obtained in the previous cycle. This leads to gradual rather than abrupt changes that can cause transients in power supply systems. An under-voltage lockout could be built into a digital controller that can monitor the primary current until it has reached a level that is sufficient to power the load, before restoring power to the load. If this is not done, the load will experience unacceptable transients as the power is switched on and off repeatedly.

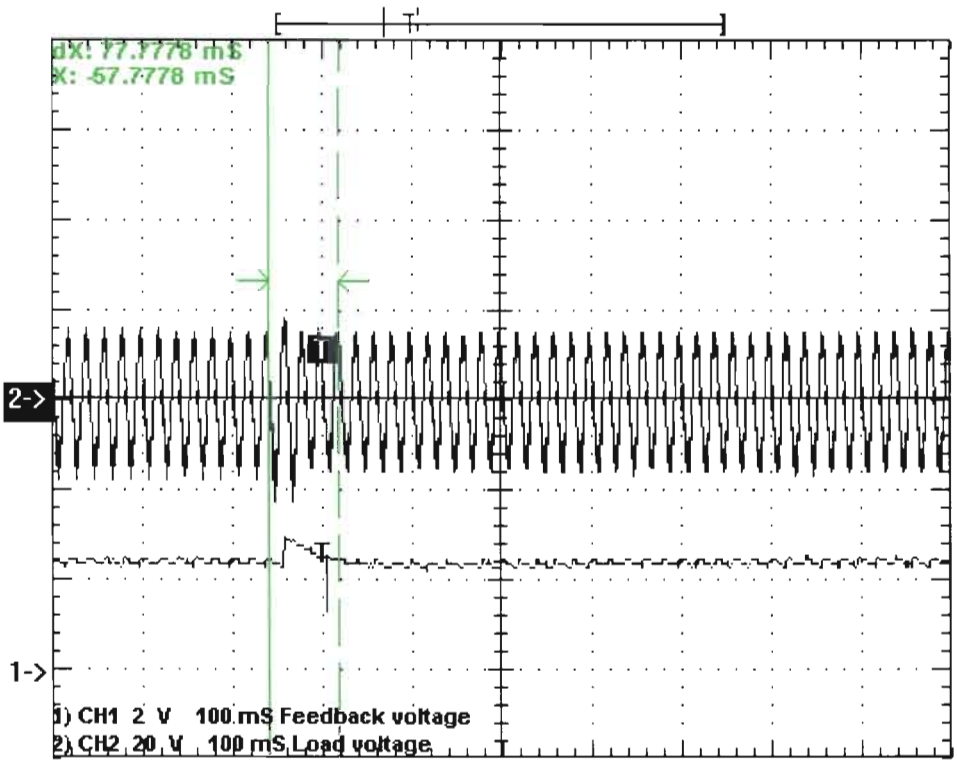


Figure 66: PID action with a load step decrease

The measurement shown in Figure 66 indicates how the PID controller brings the load voltage back to its set point value in four cycles (80 ms). The two green cursor lines highlight the area of interest. A load consisting of a resistor of 430 Ω was connected in parallel with a 180 Ω resistor. At the first cursor line the 180 Ω resistor was removed from the circuit. The trace from channel 2 shows that the load voltage increases for three half cycles before being brought back to the nominal value that it was before the step load change. The PID controller only detects the load voltage change at the first positive peak of the load voltage after the step. This can be seen in the trace of channel 1, which shows the step in load voltage to coincide with the first positive peak of the load voltage after the left-hand green cursor. The fast action of the controller to reduce the error to zero is indicated by the relatively short duration of the spike in the trace of channel 2. It measures about three cycles (60 ms). The load current changed by a factor of 3,4. The controller action under these

circumstances is acceptable.

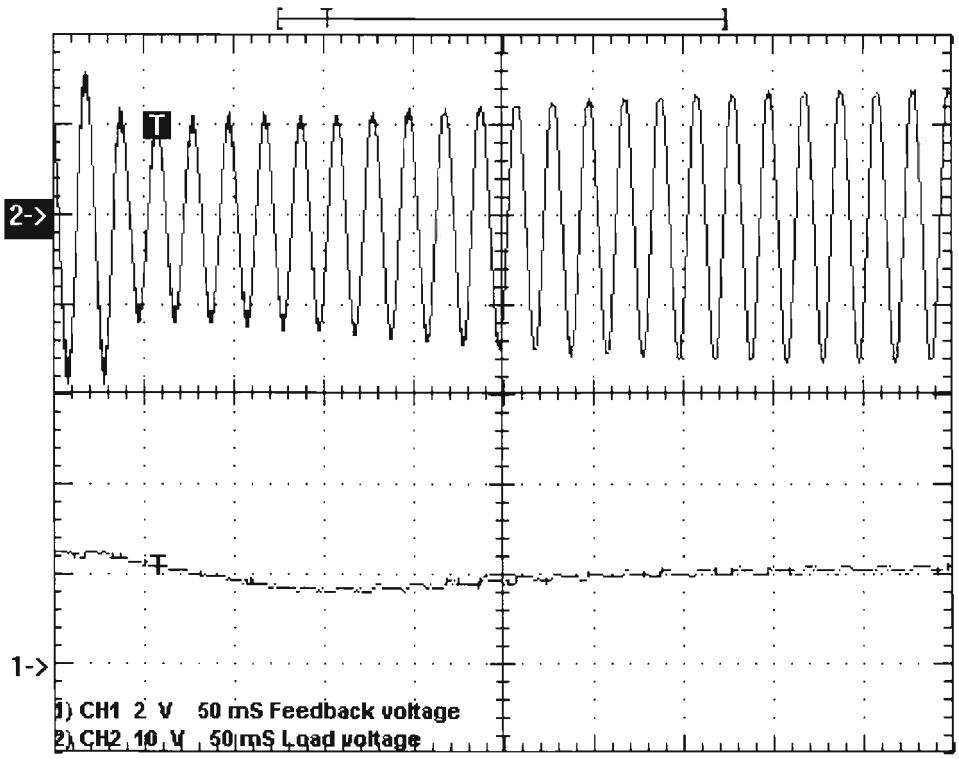


Figure 67: PID action with a load step increase

Increasing the load current with a factor of 3,4 does not have such a fast response (Figure 67). This is due to the method used to sample the peak values of the load voltage. The time constant of the capacitor and voltage divider circuit causes a gradual change in the feedback voltage. The error gradually increases as the capacitor slowly discharges over time as each positive peak is lower than the capacitor voltage and thus not forward-biasing the diode. The nature of a PID controller is to react slowly to a small error and fast to a large error. A software algorithm, which detects the peaks and holds the value until the next peak, could be used to provide a better response. The circuit would not have a capacitor to sample and hold the peak values as used in this circuit, but would often sample a rectified signal representing the load voltage, regularly updating the peak value every cycle. This would produce a fast reaction in the PID controller, similar to that seen when

the load voltage increased after a load step decrease.

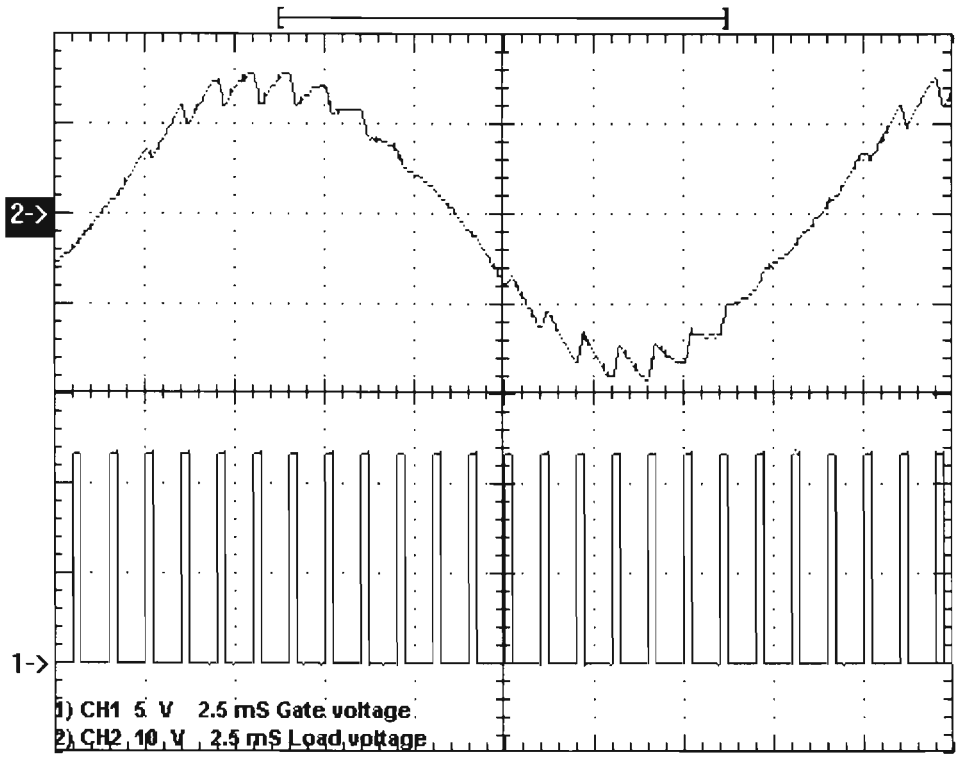


Figure 68: Load voltage and gate voltage with a reduced CT primary current

Reducing the CT primary current means that the main switch duty cycle has to be reduced in order to provide the same power per switching cycle to the load. A comparison of Figure 63 where the CT primary current was 4,5 A with Figure 68 where the CT primary current was 1 A, shows a reduction in the duty cycle of the main switch with reduced CT primary current. The voltage is essentially the same in both figures.

The voltage waveform over the main switch is shown in Figure 69. Comparison of this voltage waveform measured in the experimental set-up with that of the simulated current waveform in Figure 54 shows confirmation between the simulations and the experimental model. When the voltage is low over a switch, the current must be flowing through it and visa versa.

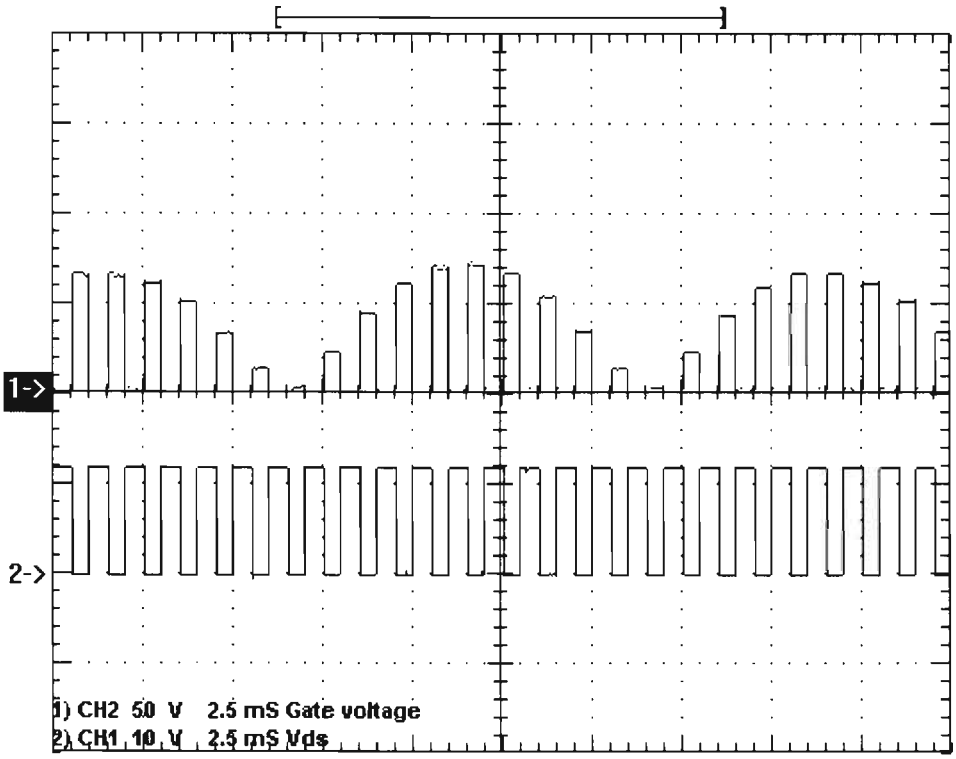


Figure 69: Main switch drain to source and gate voltages

5.3 Summary

The experimental results of two models of converting an alternating current source to a voltage were presented. The measurements were interpreted and comparisons were made between the experimental results and the simulations of the previous chapter. The confirmation between the mathematical models, simulation models and experimental models are sufficient to show beyond doubt that further research to apply these models to a high voltage system could result in a viable system.

Chapter 6 Discussion, conclusions and recommendations

6.1 Discussion

The work has been hampered by the fact that it is difficult to find a stiff source of alternating current. A stiff source of alternating current can be defined as a constant current source for AC. Varying the load should not have an influence on the magnitude of the current flowing. The only real solution would be to have access to a very high amplitude alternating voltage source with a high power rating such as is found in electric utilities. Many experiments were done and simulations which proved that this was the only alternative. To step up current means to step down voltage. This means that the voltage reflected into the primary circuit of the current transformer became significant when compared to the main source of power, which in turn influenced the current significantly when the load on the TRAFTAP increased.

The whole premises of this research has been that to draw a small percentage of power in series from a transmission line would have negligible effect on the consumers situated on the receiving end of the transmission line. This implies a transmission line voltage of 400 kV or higher and nominal currents of 500A. Parasitic power consumption of 2 kVA on a 200 MVA line would be insignificant. Even if this would increase a hundred fold it would still be insignificant.

Getting access to the utility network while no high-voltage high-power CT yet exists, is an obstacle that first has to be overcome before the "final" chapter in this research can be written.

6.2 Conclusions

Despite the limitations and drawbacks discussed above, the compatibility of the mathematical models, simulations and experimental results done in this study,

suggest that it is possible to draw significant power from a CT.

6.1 Recommendations for future work

Future research could be done on the following:

- A three-phase system of the TRAFTAP1.
- A three-phase system of the TRAFTAP2.
- Design and construction of a high-voltage current transformer with a greater than 2 kVA power rating.

Bibliography

ADDOWEESH, K.E. 1993. *An exact analysis of an ideal static AC chopper.* International Journal of Electronics Vol. 75, No. 5. Taylor & Francis Ltd.

AGRAWAL, J.P. 2001. *Power Electronic Systems: Theory and Design.* Prentice-Hall.

BROSAN, G.S.& HAYDEN, J.T. 1966. *Advanced Electrical Power and Machines.* Sir Isaac Pitman & Sons Ltd: London.

CASE, M.J. 1980. *A Direct A.C. to A.C. Regenerative Frequency and Voltage Converter.* PhD Thesis University of Cape Town.

CONNER, F.R. 1972. *Signals.* Edward Arnold (Publishers) Ltd.

CONNER, F.R. 1973. *Modulation.* Edward Arnold (Publishers) Ltd.

DUDRÍK, J. 2001. *Power Semiconductor Devices.* Mecury-Smékal. Slovakia: Kosiće.

ERICKSON, R.W. & MAKSIMOVIĆ, D. 2001. *Fundamentals of Power Electronics.* 2nd ed. Kluwer Academic Publishers.

GRIGSBY, L.L. 2001. *The Electric Power Engineering Handbook.* CRC Press.

IBRAHIM, D. 2002. *Microcontroller based temperature monitoring and control.* Newnes.

JANSE VAN RENSBURG, J.F. & CASE, M.J. 2001. *Current transformer-fed power supply.* EDPE Conference. Podbanske: Slovakia.

JENKINS, D.J. 1967. *Introduction to Instrument-Transformers.* George Newnes Limited. Londen.

LATEGAN, R. & SWART, P.H. 2001. *Standardization of Reactive Components for Drawing Power from the Shield-wire of Extra High Voltage Lines.* CIGRE Conference. Somerset West: South Africa.

MARSHALL, G.J. 1980. *Principles of Digital Communications.* McGraw-Hill Book Company.

MAZDA, F. 1997. *Power Electronics Handbook.* 3rd ed. Newnes.

MITCHELL, D.M. 1988. *DC-DC Switching Regulator Analysis.* McGraw-Hill Book Company.

MOHAN, N., UNDELAND, T.M. & ROBBINS, W.P. 2003. *Power Electronics, Converters, Applications and Design.* 3rd ed. John Wiley and Sons.

NISE, N.S. 2000. *Control Systems Engineering.* 3rd ed. John Wiley & Sons, New York.

RASHID, M.H. 2004. *Power Electronics, Circuits, Devices and Applications.* 3rd ed. Prentice Hall.

TRAISTER, J.E. 1983. *Handbook of Power Generation: Transformers and Generators.* Prentice-Hall, New York.

VARENNES, L.B. 2001. *IVACE is integrated into the microwave network.* HydroTech Vol. 14, No. 1 Spring-Summer 2001, www.ireq.ca.

STUBBS, L. 1994. *Tapping power from high voltage transmission lines using insulated lightning shield wires and series compensation.* Thesis for Master of

Science in Engineering: Witwatersrand University: Johannesburg.

UNITRODE. 1999. *UC3842/3/4/5 Provide Low-cost Current-Mode Control.* Unitrode Application Note U-100A.

ANNEXURE A MATLAB PROGRAM

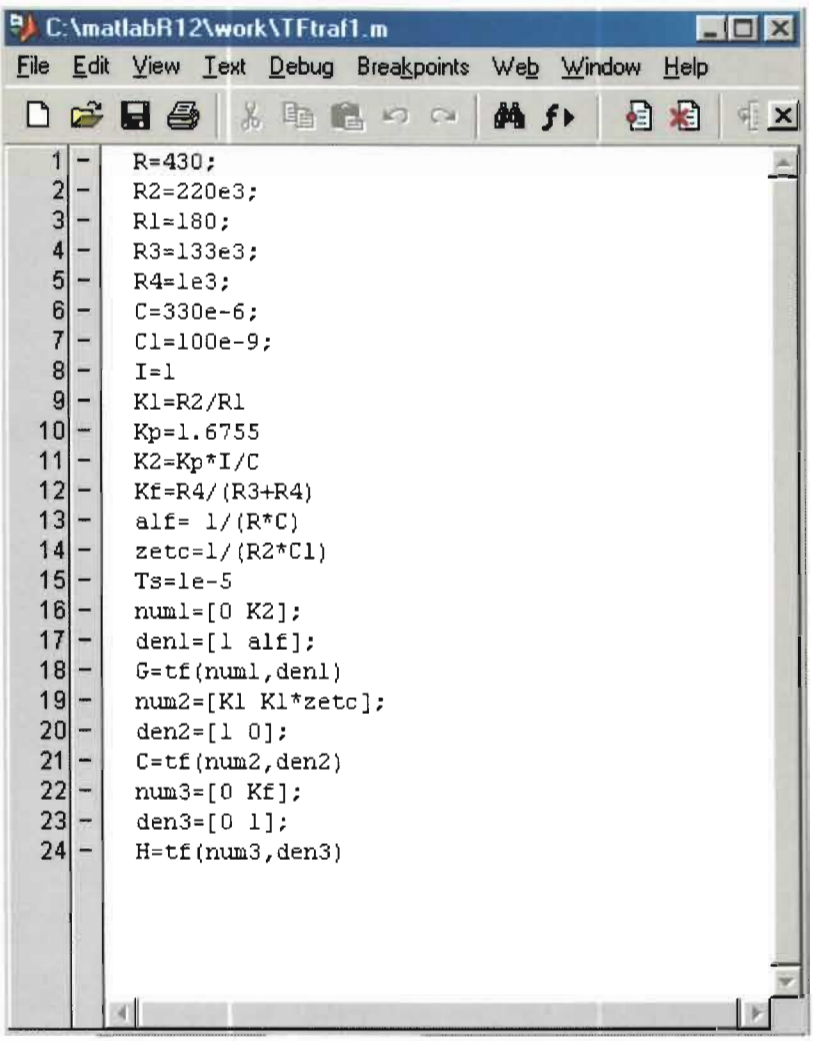


Figure 70: Screen snapshot of MATLAB program to evaluate transfer functions

ANNEXURE B C-PROGRAM FOR PID CONTROLLER

```
/*****************************************************************
*   PROJECT: PID algorithm implemented for control of TRAFTAP2
*   DATE:  9 Oct 2005
*   FILE: PID.C
*   PROCESSOR: 18F452 / 16F874
*   COMPILER: CCS PIC C
*   PROGRAMMER: J F Janse van Rensburg
*   REFERENCE: (Ibrahim  2002:217)
*****************************************************************/
#include <18F452.h>                 // change to 16F874 if using PIC16F874
#device ADC=10                      // 10 bit A/D
#fuses XT,NOWDT,NOPROTECT,NOLVP,NOBROWNOUT
#use delay(clock=4000000)

void main()
{

/* Declare the variables */

float a,b,c,T,T1,Ti,Tdl,K,Kp,SetPoint,rkt,LSB,ekt,pkt,qkt,ykt,ukt;
float MAX,MIN,pkt1,ekt1,Duty;
long DutyCycle;
long int V0;

/* Initialize the peripherals */

  setup_adc_ports(RA0_ANALOG);
  setup_adc(ADC_CLOCK_INTERNAL);
  set_tris_A( 0b11111111 );
```

```
  setup_psp(PSP_DISABLED);
  setup_spi(FALSE);
  setup_counters(RTCC_INTERNAL,RTCC_DIV_2);
  setup_timer_1(T1_DISABLED);
  setup_timer_2(T2_DIV_BY_4,249,1);
  setup_ccp1(CCP_PWM);
  setup_ccp2(CCP_PWM);

/* Assign initial values to variables */

  LSB = 5.0/1024.0;              // floating point needs decimal point
  MIN = 0.0;
  MAX = 1000.0;
  pkt1 = -150.0;                 // limits overshoot at start-up
  ekt1 = 0.0;

/* Calculate the PID parameters */

  T = 0.001;                     // 1 ms sampling time
  T1 = 0.01;                     // 10 ms rise time
  Tdl = 0.001;                   // 0,1 ms delay time
  K = 134;                       // amplitude response per unit step
  Ti = 4*Tdl;                    // integral time constant
  Td = 0.5*Tdl                   // differential time constant
  Kp = 3*T1/(K*Tdl);             // proportional gain
  a = Kp;
  b = Kp*T/Ti;
  c = Kp*Td/T;

/* Set point given in volts for 332.5 V output = 235 V rms  */

  SetPoint = 2.5;
```

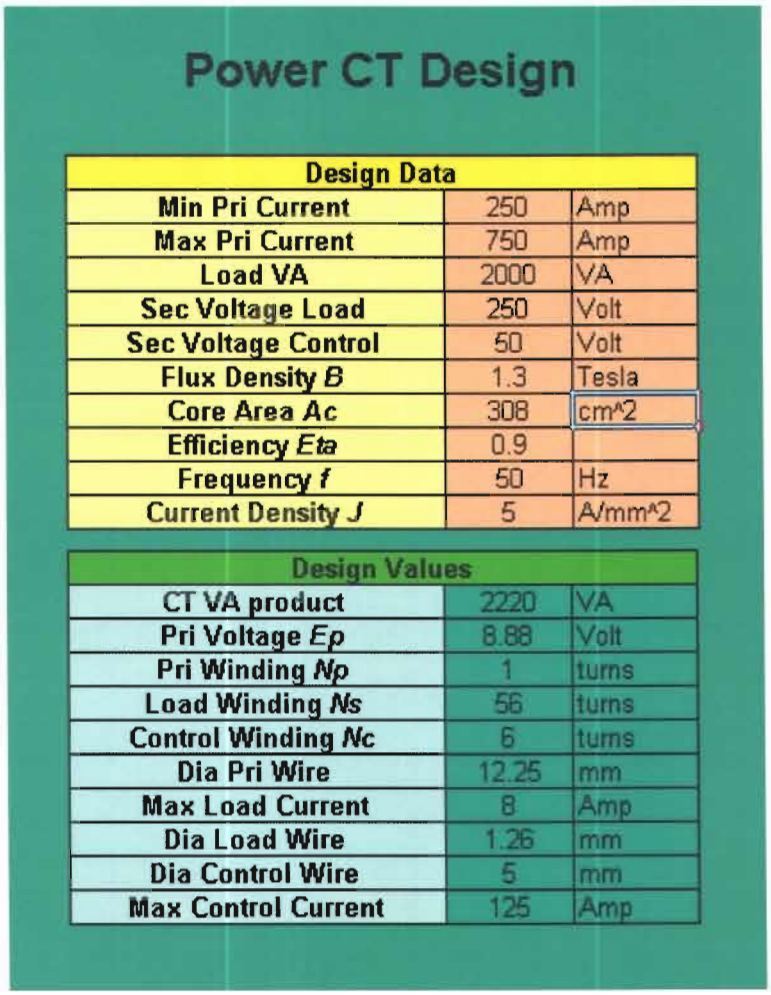
```
/* Soft-start routine */

  Duty = 330.0;                  // start up with a limited duty cycle
  DutyCycle = (long)Duty;        // Convert to integer
  set_pwm1_duty(DutyCycle);      // Implement soft start duty cycle
  delay_us (55000);              // for 55 ms


/* Start PID control loop  */

  while(1)                       // Do forever ...
  {

/* Do A/D conversion on channel 0 and determine feedback voltage */

    set_adc_channel( 0 );        // Do A/D
    delay_us( 20 );              // wait for result to be ready
    V0 = read_adc( );            //  read A/D result
    ykt=V0*LSB;                  // Calculate feedback voltage equivalent

/* Calculate the duty cycle required */

    rkt=SetPoint;
    ekt=rkt-ykt;                 // Calculate error voltage
    pkt=b*ekt+pkt1;              // Calculate the integral term
    qkt=c*(ekt-ekt1)             // Calculate the differential term
    ukt=pkt+a*ekt+qkt;           // Calculate the PID output
    Duty = 500.0 + ukt;          // Calculate duty cycle around 50%
```

```
/* Saturate output if required */

 if (Duty > MAX)                // Output saturated?
 {
   pkt = pkt1;                  // Zero integral to prevent integral windup
   ekt = ekt1;
   Duty = MAX;                  // Duty cycle cannot be greater than 100%
 }
 else if (Duty < MIN)           // Limit Duty cycle to zero?
 {
   pkt=pkt1;                    // Zero integral to prevent integral windup
   ekt = ekt1;
   Duty=MIN;                    // Duty cycle cannot be less than 0%
 }

/* Limit any overshoot of output voltage to a safe value */

 if ( Duty = = MAX)             // Limit overshoot at start-up
 {
   if (ekt < 0.0)
   {
    Duty=500.0;
    pkt = -250;
    ekt = ekt1;
   }
 }

 if ( V0 > 580 )                // Limit any high voltage surges
 {
   pkt = -150;
 }
```

```
/* Apply duty cycle to circuit */

    DutyCycle=(long)Duty;          // Convert to integer
    set_pwm1_duty(DutyCycle);      // Update duty cycle
    pkt1=pkt;
    ekt1=ekt;
    delay_us( 500 );               // Wait out sampling time
  }                                // Repeat the control loop
}                                  // End
```

ANNEXURE C POWER CT DESIGNER

A spreadsheet calculator with a user-friendly interface was designed. The interface is shown in Figure 71.



Power CT Design

Design Data		
Min Pri Current	250	Amp
Max Pri Current	750	Amp
Load VA	2000	VA
Sec Voltage Load	250	Volt
Sec Voltage Control	50	Volt
Flux Density *B*	1.3	Tesla
Core Area *Ac*	308	cm^2
Efficiency *Eta*	0.9	
Frequency *f*	50	Hz
Current Density *J*	5	A/mm^2

Design Values		
CT VA product	2220	VA
Pri Voltage *Ep*	8.88	Volt
Pri Winding *Np*	1	turns
Load Winding *Ns*	56	turns
Control Winding *Nc*	6	turns
Dia Pri Wire	12.25	mm
Max Load Current	8	Amp
Dia Load Wire	1.26	mm
Dia Control Wire	5	mm
Max Control Current	125	Amp

Figure 71: Screen snapshot of Power CT designer

ANNEXURE D PHOTO'S

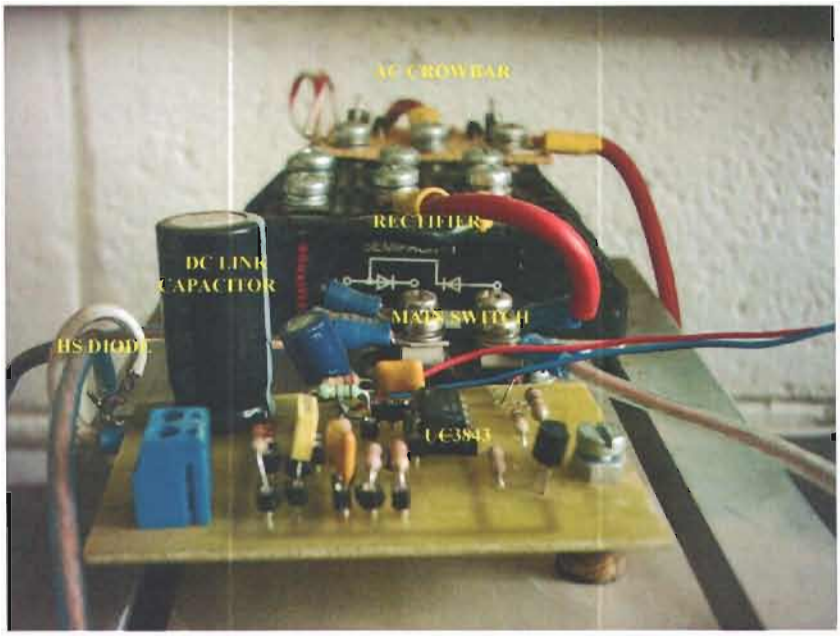


Figure 72: TRAFTAP1 experimental circuit

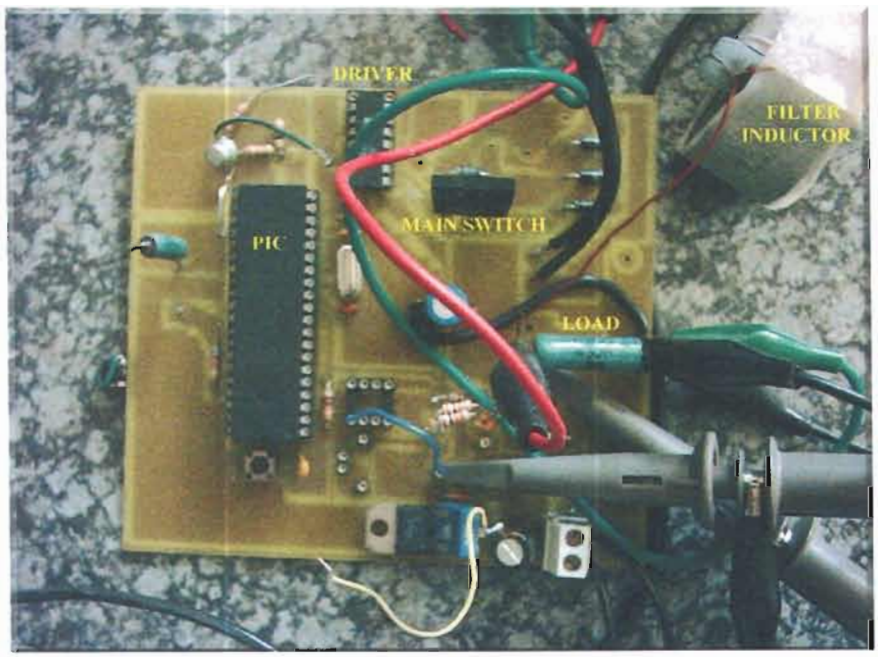


Figure 73: TRAFTAP2 experimental circuit

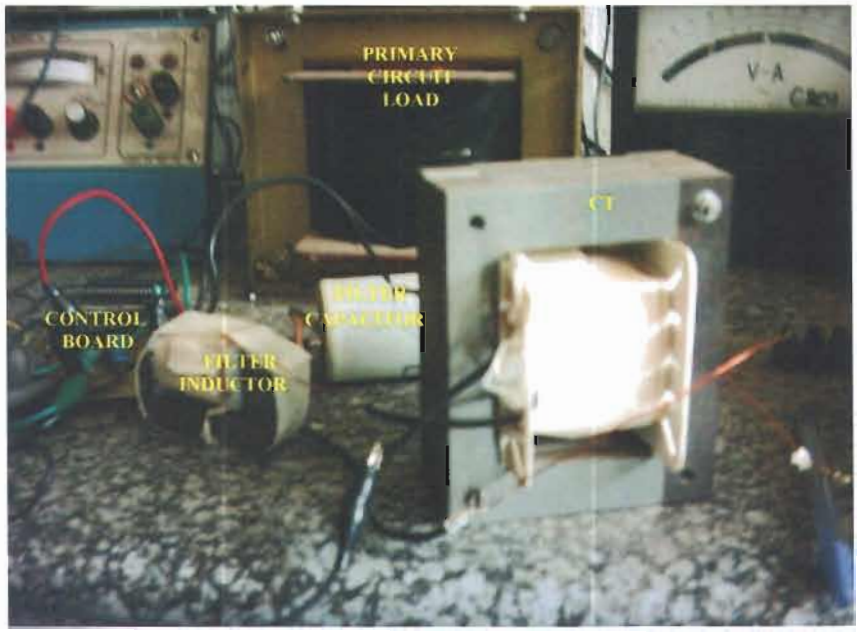


Figure 74: Components of TRAFTAP2 experimental set-up

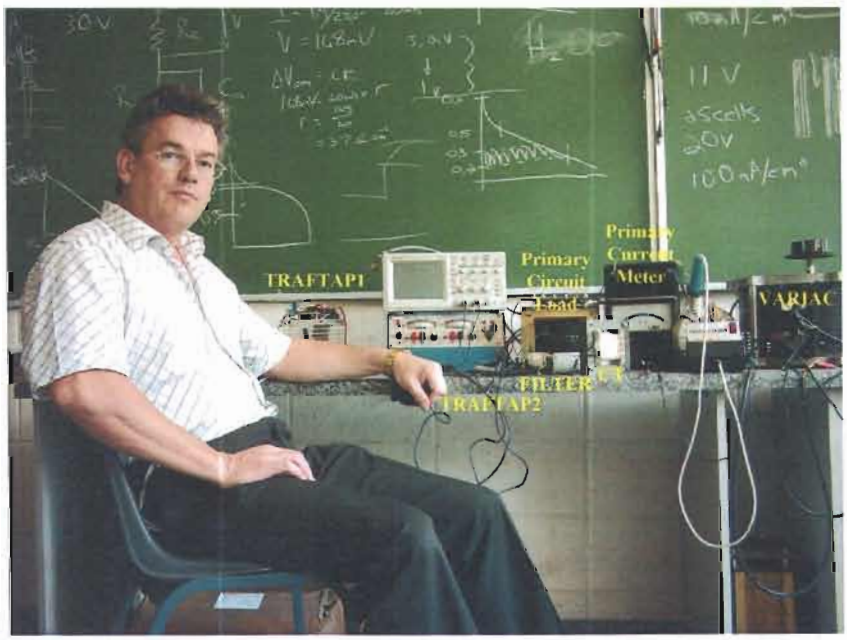


Figure 75: In the laboratory with TRAFTAP1 and TRAFTAP2 models

This D-degree is not caffeine-free.